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CHAPTER 3. CONTROL IN POWER ELECTRONIC CIRCUITS

Alternated duty cycle control method for half-bridge DC-DC converter

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Abstract

A control method, namely, Alternated Duty Cycle (ADC) control, is presented in this paper. This method can achieve soft-switching for at least one switch of the two half-bridge switches. When soft-switching can be achieved only for one switch, ADC control alternates the soft-switching realization between the two switches so that each switch will be soft-switched during half of the time and hard-switched during the other half, keeping equal power losses distribution between the switches for better thermal management. Moreover, any asymmetry in the duty cycle will not cause asymmetric components stresses or transformer DC bias when ADC control is used. Theoretical analysis and implementation are presented along with experimental results.

1 Introduction

Half-bridge topology [1-3] can be a good candidate for high power density DC-DC conversion, especially in those applications that use Point-Of-Load

(POL) DC-DC converters for present and future generation of ICs (Integrated Circuits). This is because of several reasons including structure simplicity, lower number of switches, lower isolation transformer primary side turns since half of the input voltage is applied to the transformer windings, and possibility to achieve soft-switching with the appropriate control [1-3]. There are two main conventional control schemes used in the half-bridge topology. One is the conventional symmetric PWM control and the other is the asymmetric (complementary) control [1,2] where two driving signals are complementarily generated.

The switching frequency continues to increase mainly to reduce the size and cost of passive components and to improve the dynamic performance [3-4]. Hence, soft-switching techniques become more desirable in order to reduce the increased switching losses and switches body diodes reverse recovery losses at increased switching frequencies [1-3,5,6].

When the conventional symmetric control is used for a half-bridge, its two switches operate at hard-switching, while when the asymmetric (complimentary) control is used, the two half-bridge switches operate at soft-switching, but unfortunately, causing asymmetric stresses on the converter components which is not desirable especially for wide input voltage range, say 35V∼75V or 300V∼400V [1-3]. Moreover, the DC gain is not linear which degrades the converter performance. In this paper, a control method, namely, Alternated Duty Cycle (ADC) control, is presented. This method can achieve soft-switching for at least one switch of the two half-bridge switches. When soft-switching is only achieved for one switch, ADC control alternates the soft-switching realization between the two switches so that each switch will be soft-switched during half of the time and hard-switched during the other half, keeping equal power losses distribution between the switches. Moreover, any asymmetry in the duty cycle will not cause asymmetric components stresses when ADC control is used.

The next section briefly presents the Alternated Duty Cycle (ADC) control and its principle of operation followed by a theoretical analysis and comparison in Section 3. Section 4 discusses the experimental work. The conclusion is given in Section 5.

2 Alternated duty cycle control and principle of operation

This section briefly discusses what it meant by the Alternated Duty Cycle (ADC) control before going into the details and ADC configurations descrip-

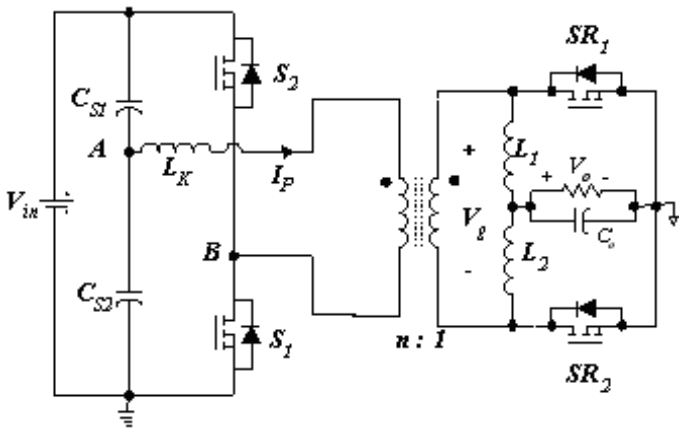

Figure 1: Half-bridge topology with current doubler secondary side.

tion when applied to half-bridge converter, such as the one shown in Fig. 1 along with its modulation scheme and modes of operation.

2.1 Basic concept of the alternated duty cycle control scheme

Let us assume two arbitrary waveforms, C_a and C_b, generated from the PWM controller for the half-bridge as shown in Fig. 2, where T_s is the switching cycle period, D is the switching duty cycle or ratio, and m is a real number (can be floating number). When $m = 1$, C_a and C_b become the control signals of asymmetric control, and when $m = (1 - D)/D$, C_a and C_b become the control signals of symmetric control.

C_1 and C_2 in Fig. 2 are the ADC control waveforms to drive S_1 and S_2, respectively, where C_a and C_b ON times are alternated between the two switches so that S_1 will be turned ON by $C_a$in the first cycle and by C_b in the following cycle and vise versa for S_2, resulting in C_1 and C_2.

When C_a and C_b are the asymmetric control signals (at $m = 1$), the resulting ADC control signals C_1 and C_2 will result in symmetric voltages across the half-bridge capacitors C_{S1} and C_{S2} even though the duty cycle is asymmetric since the average duty cycles of C_1 and C_2 are symmetric. This will result in a converter that works but, unfortunately, lacks the ability to be regulated for the output voltage at different input and output conditions. The reason for this phenomenon is that in order to have the regulation ability in the half-bridge converter, switching dead time period is required as in the symmetric control or asymmetry is required as in asymmetric control, which

is lost in this case.

Under this condition, when $m = 1$, this topology is suitable for applications where intermediate "DC transformer" is required, and regulation is not required.

Therefore, m will be larger than one resulting in losing the soft-switching operation for one switch. However, it is interesting to note that the soft-switching will be "alternated" between the two half-bridge switches, i.e., S_1 will be soft-switched in the first cycle and hard switched in the following cycle and so on, and vise versa for S_2. When $m = (1 - D)/D$, symmetric (equal) duty cycles are achieved for C_a and C_b and hence for C_1 and C_2. However, in the ADC control, equal duty cycle is not required since it will not affect the symmetry of the converter.

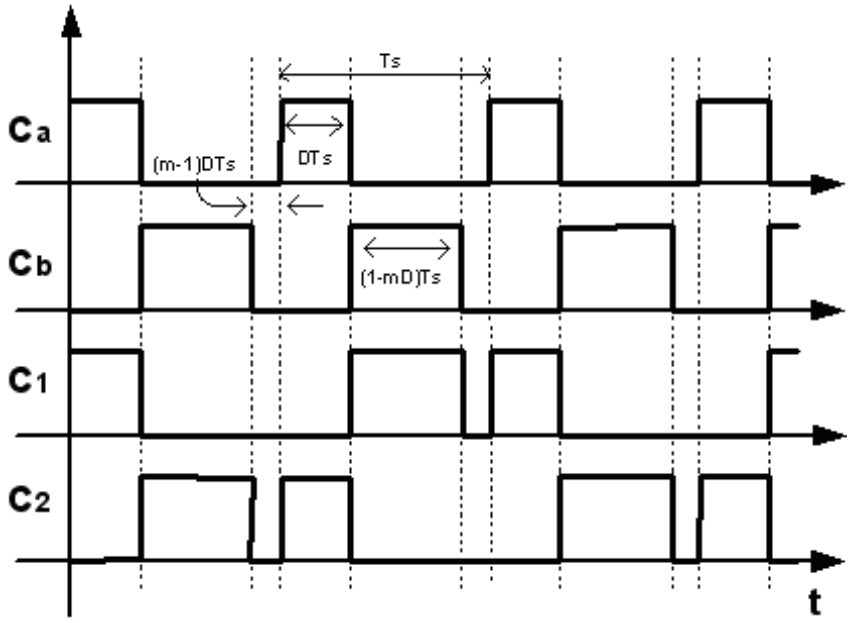

Figure 2: Generalized alternated duty cycle control waveforms.

2.2 ADC PWM modulation

Different modulation schemes can be adapted to generate the ADC control signals. ADC modulation can be digital modulation or analog modulation. In digital modulation case, it is generally simple to generate any, even complicated, control signals such as those required for ADC control. For the

case of analog modulation for ADC control, Fig. 3 shows a possible modulation approach for the realization of ADC PWM control. $V_{sawtooth}$ is the modulation carrier waveform, and V_c is the main control voltage derived from the voltage or current controller/compensator, from which the other control voltage $V_p - mV_c$ is generated, where V_p is the peak voltage of the

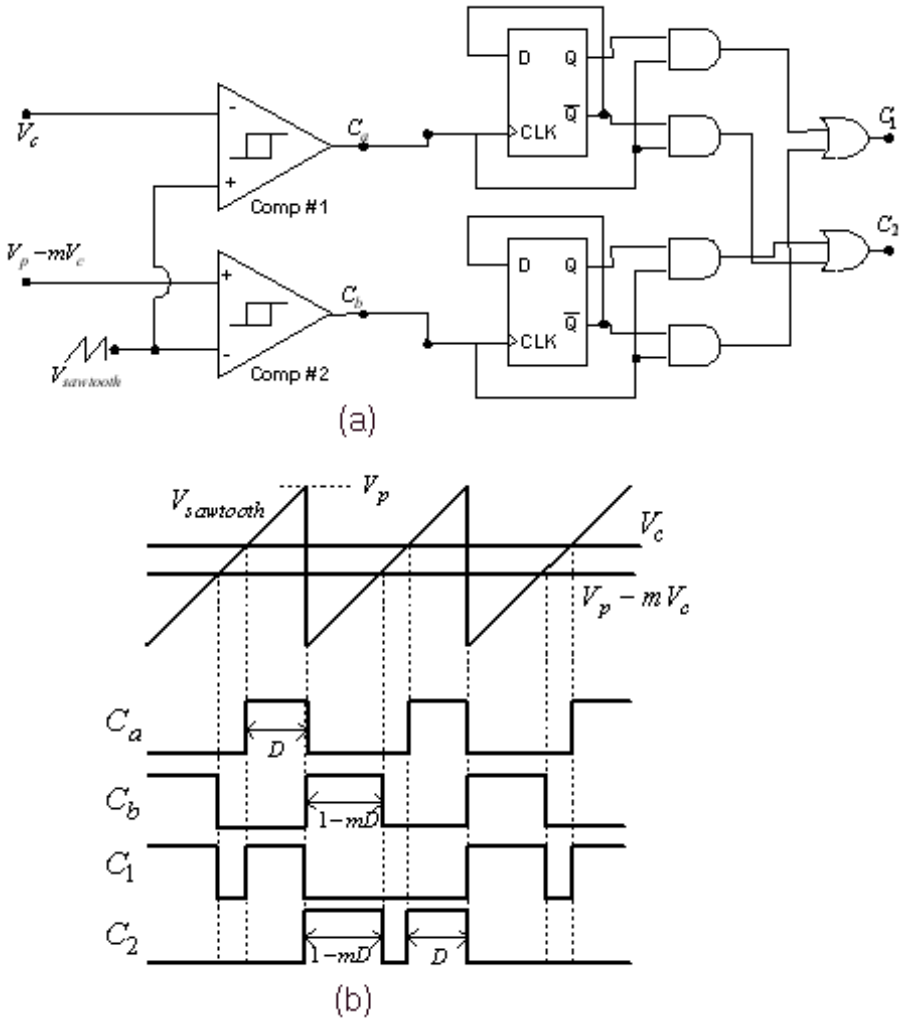

Figure 3: A PWM modulation scheme for Alternated Duty Cycle control: (a) modulation circuit, and (b) modulation waveforms.

carrier $V_{sawtooth}$. By modulating V_c and $V_p - mV_c$, the signals C_a and C_b can be generated, from which the final half-bridge switches control signals, C_1 and C_2, are then generated using a logic stage that consists of D-flip-flops, AND, and OR logic gates, as shown in Fig. 3.

2.3 Modes of operation

Figure 4 shows the theoretical main switching waveforms of the ADC controlled half-bridge of Fig. 1. The main modes of operation can be summarized as follows:

Mode 1 ($t_0 < t < t_1$): S_1 is ON and S_2 is OFF during this mode starting $t = t_0$, and the input power is being delivered to the output through $L_1$and SR_2 which is also ON during this mode (SR_1 is OFF). During this mode, L_1 is charged and L_2 freewheels (discharges) through SR_2. This mode last for a duration of $(1 - mD)T_s$, where $1 < m < 1/D$.

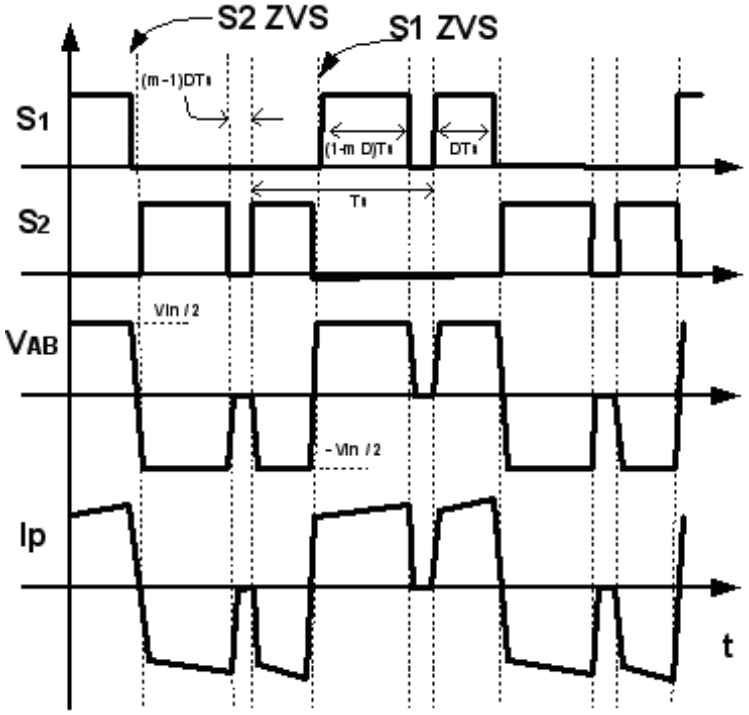

Figure 4: ADC controlled half-bridge main switching waveforms.

Mode 2 $(t_1 < t < t_2)$: S_1 is turned OFF at $t = t_1$ and SR_1 and SR_2 are turned ON, causing the primary current I_P to charge S_1 junction capacitance C_{j1} and discharge C_{j2}. When the secondary side switches SR_1 and SR_2 start to freewheel, the isolation transformer leakage inductance L_K and the primary side switches' junction capacitances, C_{j1} and C_{j2}, oscillate on the primary side.

Mode 3 $(t_2 < t < t_3)$: At $t = t_2$, S_1 is turned ON again. This mode is similar to Mode 1 except that it lasts for duration of DT_s.

Mode 4 $(t_3 < t < t_4)$: S_1 is turned OFF at $t = t_3$, causing the primary current I_P to charge C_{j1} and discharge C_{j2}. During this Mode, the reflected secondary inductor current dominates the primary current I_P. Therefore, the voltage across C_{j2} may be discharged to zero, which provides wide Zero-Voltage-Switching (ZVS) condition for S_2.

Mode 5 $(t_4 < t < t_5)$: At $t = t_4$, S_2 is turned ON with ZVS. SR_1 is ON and SR_2 is OFF. During this mode and the input power is being delivered to the output through L_2 and SR_1. L_2 is charged and L_1 freewheels (discharges) through SR_1. This mode last for duration of $(1 - mD)T_s$.

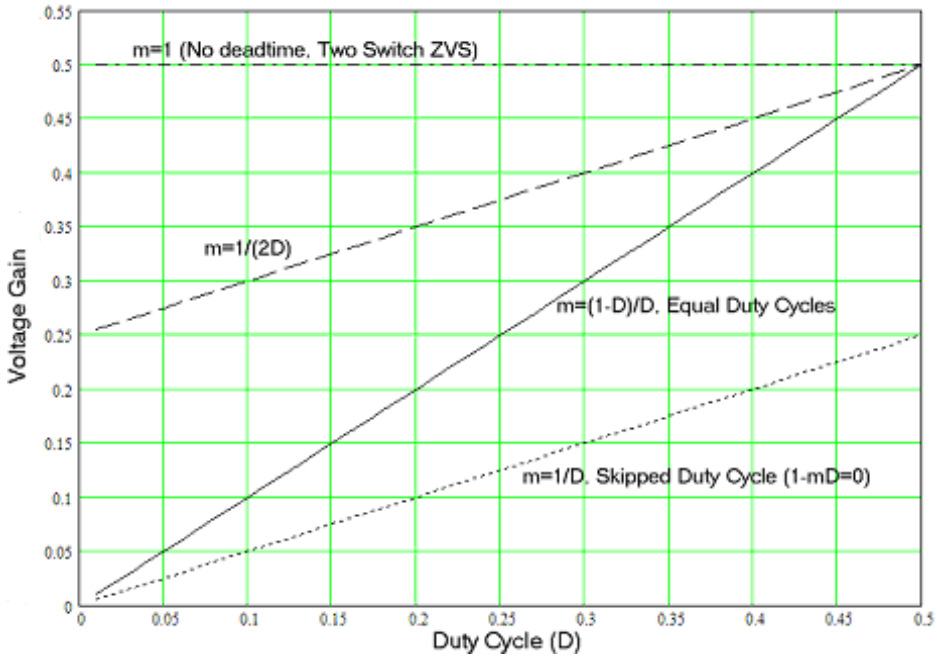

Figure 5: Voltage gain versus duty cycle for different values of m.

Mode 6 ($t_5 < t < t_6$): S_2 is turned OFF at $t = t_5$ and SR_1 and SR_2 are turned ON, causing the primary current I_P to charge C_{j2} and discharge C_{j1}. When the secondary side switches SR_1 and SR_2 start to freewheel, the isolation transformer leakage inductance L_K and the primary side switches' junction capacitances, C_{j1} and C_{j2}, oscillate on the primary side.

Mode 7 ($t_6 < t < t_7$): At $t = t_6$, S_2 is turned ON again. This mode is similar to Mode 5 except that it lasts for duration of DT_s.

Mode 8 ($t_7 < t < t_8$): S_2 is turned OFF at $t = t_7$, causing the primary current I_P to charge C_{j1} and discharge C_{j2}. During this Mode, the reflected secondary inductor current dominates the primary current I_P. Therefore, the voltage across C_{j1} may be discharged to zero, which provides wide ZVS condition for S_1. After this, Mode 1 starts again by turning ON S_1 with ZVS.

From Fig. 4 and the modes of operation analysis, it can be noticed that when the falling edge of one switch gate signal is close to the rising edge of the rising edge of the other switch, ZVS is achieved for the other switch by utilizing the leakage inductor stored energy. ZVS is achieved alternatively for the two half-bridge switches.

3 Theoretical analysis and comparison

It can be shown by simply applying the volt-second-balance across the output inductors that the voltage gain equation for the ADC controlled half-bridge is given by:

$$\frac{V_o}{V_g} = \frac{1 - D(m-1)}{2} \text{ or } \frac{V_o}{V_{in}} = \frac{1}{4n} \cdot [1 - D(m-1)], 1 < m < \frac{1}{D} \quad (1)$$

which means that:

$$D = \frac{V_g - 2V_o}{V_g(m-1)}. \quad (2)$$

Fig. 5 shows the voltage gain versus duty cycle for different values of m. The output current ripple equation is given by:

$$\Delta I_o = \frac{2 \cdot V_o}{L \cdot f_s} \cdot D(m-1) = \frac{2V_o}{V_g} \frac{V_g - 2V_o}{L \cdot f_s}, \quad (3)$$

$V_g = \frac{V_{in}}{2n}$ for ADC controlled half-bridge.

Fig. 6 shows the output current ripple versus duty cycle from Eq. (3) for $V_o = 3.3$V, $L = 2\mu$H, and $f_s = 400$kHz at different m values. It can

	Asymmetric HB	*Symmetric HB*	*ADC HB*
Soft-Switching	S_1, S_2	None	S_1 and S_2 Alternatively
Stresses	Asymmetric	Symmetric	Symmetric
DC gain	$V_{out}=\frac{D(1-D)V_{in}}{n}$	$V_{out}=\frac{DV_{in}}{2n}$	$V_{out}=\frac{V_{in}}{2n}\cdot[1-D\cdot(m-1)]$ $V_{out}=\frac{DV_{in}}{n}$, Equal D Case
DC Bias of magnetizing current	$I_{DC}=\frac{(1-2D)}{2\cdot n}I_O$	$I_{DC}=0$	$I_{DC}=0$
Stresses of switch S_1	$V_{s1}=V_{in}$, $Irms=\frac{I_o(1-D)\sqrt{D}}{n}$	$V_{s1}=V_{in}$, $Irms=\frac{I_o}{2n}\sqrt{D}$	$V_{s1}=V_{in}$, $Irms=\frac{I_o}{n\cdot 2\cdot\sqrt{2}}\sqrt{(m+1)\cdot D}$
Stresses of switch S_2	$V_{s2}=V_{in}$, $Irms=\frac{I_oD\sqrt{1-D}}{n}$	$V_{s2}=V_{in}$, $Irms=\frac{I_o}{2n}\sqrt{D}$	$V_{s2}=V_{in}$, $Irms=\frac{I_o}{n\cdot 2\cdot\sqrt{2}}\sqrt{(m+1)\cdot D}$
Stresses of rectifier SR_1	$V_{SR2}=\frac{(1-D)V_{in}}{n}$, $Irms=I_o\sqrt{1-D}$	$V_{SR1}=\frac{V_{in}}{2n}$, $I_{rms}=\frac{I_o}{2}\sqrt{2D+1}$	$V_{SR1}=\frac{V_{in}}{2n}$, $I_{rms}=\frac{I_o}{2}\sqrt{(m+1)\cdot D+1}$
Stresses of rectifier SR_2	$V_{SR1}=\frac{DV_{in}}{n}$, $I_{rms}=I_o\sqrt{D}$	$V_{SR2}=\frac{V_{in}}{2n}$, $Irms=\frac{I_o}{2}\sqrt{2D+1}$	$V_{SR2}=\frac{V_{in}}{2n}$, $I_{rms}=\frac{I_o}{2}\sqrt{(m+1)\cdot D+1}$

Table 1: A comparison/stresses of basic half-bridge converters under three control schemes.

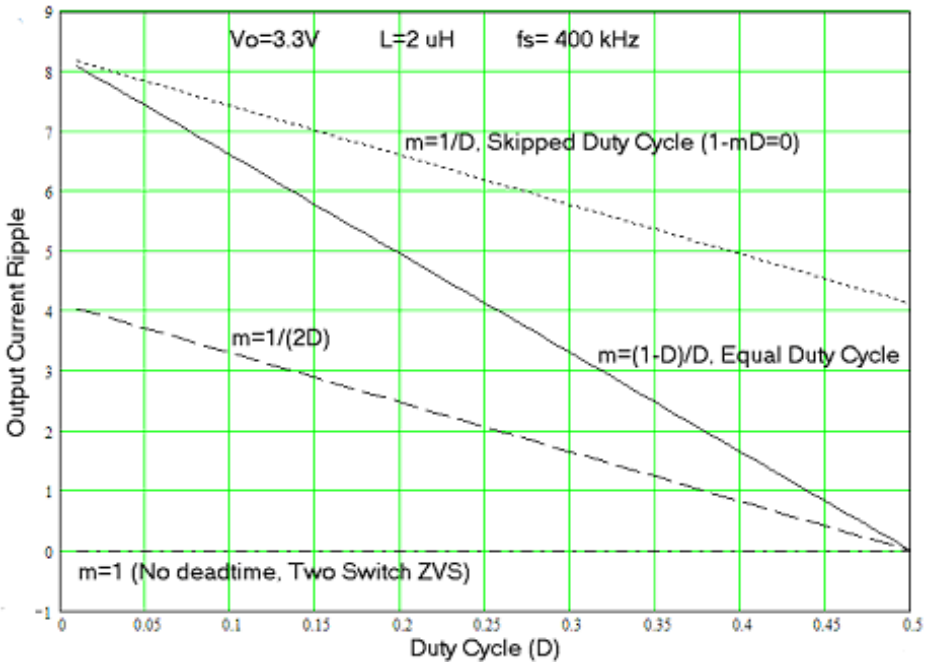

Figure 6: Output current ripple versus duty cycle at different m values for $V_o = 3.3$V, $L = 2\mu$H, and $f_s = 400$kHz.

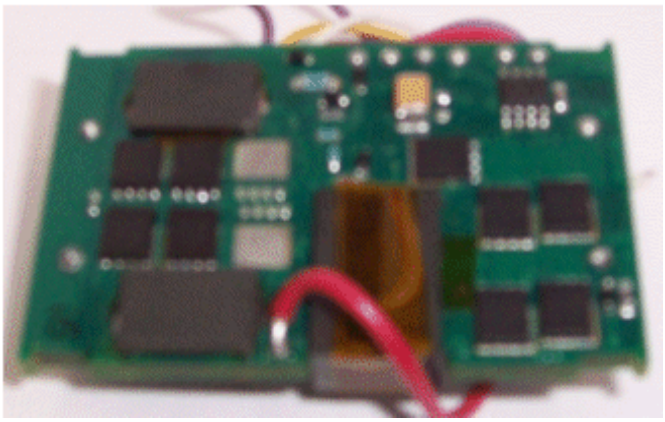

Figure 7: Photo of the half-bridge DC-DC converter prototype.

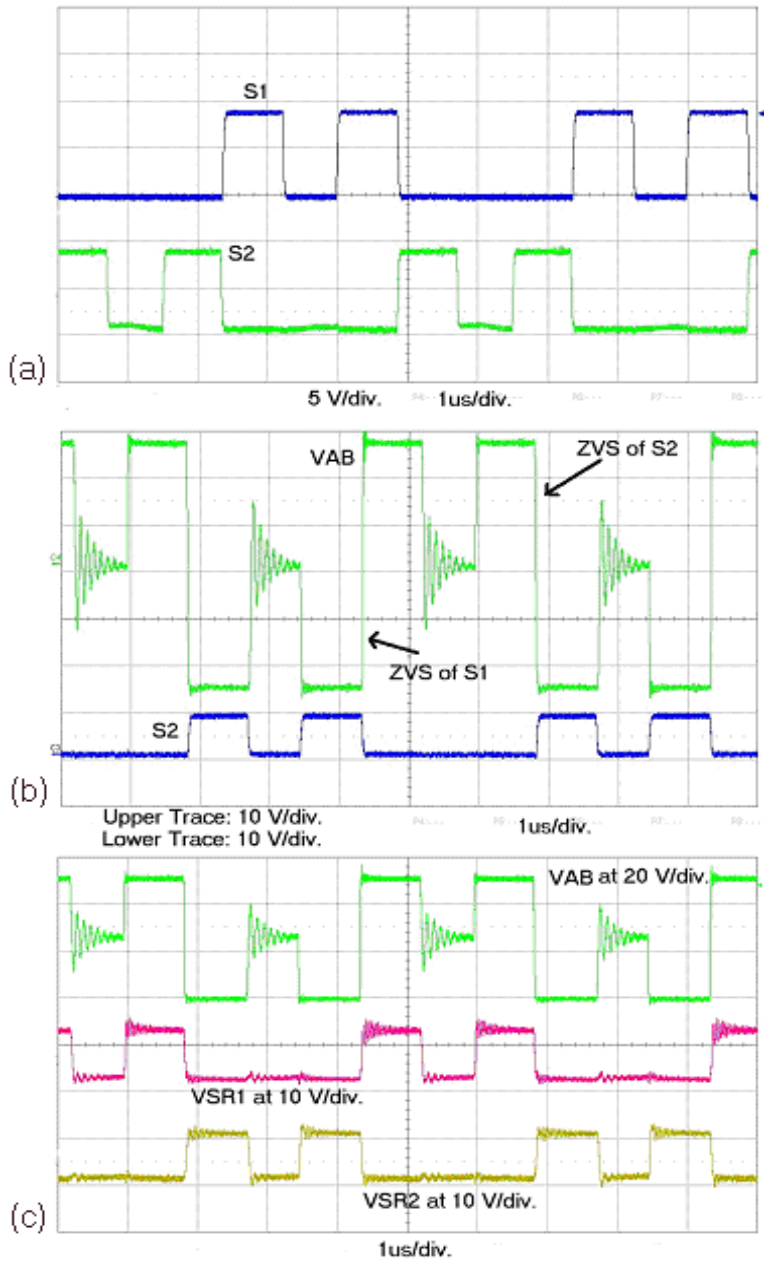

Figure 8: Experimental waveforms: (a) $S_1$and S_2 driving signals, (b) isolation transformer primary side voltage V_{AB} and S_2 driving signals, (c) isolation transformer primary side voltage V_{AB} and S_{R1} and S_{R2} drain-to-source voltages.

be noticed that as m gets smaller and approaches one, the output current ripple gets smaller and reduced.

Table 1 shows some of the characteristics/stresses of the ADC controlled half-bridge compared to other half-bridge control schemes.

4 Experimental work

A 100W half-bridge prototype of the type of in Fig. 1 and having nominal input voltage $V_{in} = 48V$ and output voltage $V_o = 3.3V$, was built in the laboratory for verification and evaluation and shown in the photo of Fig. 7. The switching frequency is 400kHz and with output inductors of $L_1 = L_2 = 500$nH. The primary side switches S_1 and S_2 are Si7456DP each. At the secondary side, synchronous rectifiers (SRs) are used, two Si7892DP paralleled in each of the two current doubler channels. The prototype is ADC controlled with equal duty cycles ($m = (1 - D)/D$). Fig. 8 shows some experimental waveforms. Fig. 8a shows the two half-bridge switches ADC gate driving while Fig. 8b shows the isolation transformer primary side voltage with one of the switches driving signal were ZVS is achieved alternatively between the half-bridge two switches. Fig. 8c shows the isolation transformer primary side voltage along with the waveforms of the SRs drain-to-source voltages. The experimental waveforms agree with the theoretical ones. Fig. 9 shows the prototype measured efficiency curve.

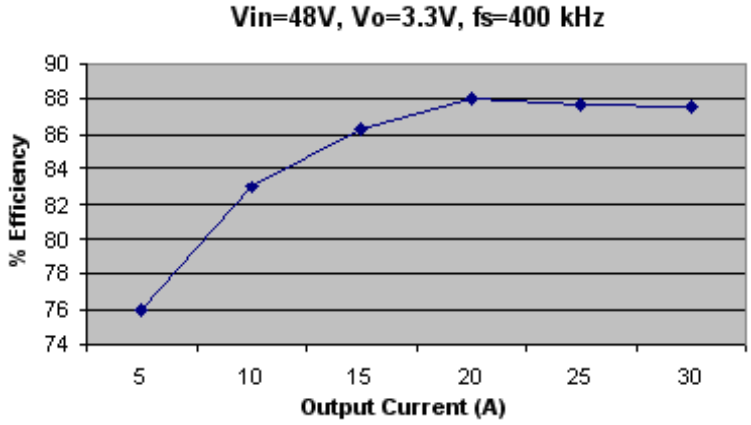

Figure 9: Experimental efficiency curve.

5 Conclusion

The Alternated Duty Cycle (ADC) control is presented in this paper. This method can achieve soft-switching for at least one switch of the two half-bridge switches. When soft-switching is achieved only for one switch, ADC control alternates the soft-switching realization between the two switches so that each switch will be soft-switched during half of the time and hard-switched during the other half, keeping equal power losses distribution between the switches and resulting in good thermal management. Moreover, the any asymmetry in the duty cycle will not cause asymmetric components stresses, DC transformer bias, or nonlinear DC gain when ADC control is used. Description and theoretical analysis and implementation were presented along with experimental results.

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References

[1] J. Sebastian, J.A. Cobos, O. Garcia, and J. Uceda, IEEE Power Electronics Specialists Conference, PESC'95, p.1229 (1995).

[2] P. Imbertson and N. Mohan, IEEE Transaction on Power Electronics **29**, 121 (1993).

[3] Y. Panov and M. Jovanovic, IEEE Fourteenth Annual Applied Power Electronics Conference and Exposition, APEC'99, vol. **1**, p.545 (1999).

[4] J.A. Abu-Qahouq, Hong Mao, and I. Batarseh, IEEE 33-rd Annual Power Electronics Specialists Conference, PESC'02, vol. **4**, p.1576 (2002).

[5] R. Redl, N.O. Sokal, and L. Balogh, IEEE Power Electronics Specialists Conference PESC'95, p.162 (1990).

[6] G.A. Karvelis, M.D. Manolarou, P. Malatestas, and S.N. Manias, IEE Proc. Electric Power Applications **148**, 419 (2001).