

Towards an on-chip boost switching power converter: a design space exploration

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Abstract

This work presents the design space exploration of a boost switching power converter focused on its monolithic implementation. An analysis in terms of the models of its main circuit elements (switching transistors, inductor, and capacitor) is described. The figure of merit is defined taking into account output voltage ripple, power efficiency, and occupied die area as performance indexes, from which a singular point that maximizes performance is obtained. Transistor-level simulation results for a particular 0.35 μm standard CMOS technology are presented to validate the approach.

1 Introduction

The thrust for miniaturization of power supplies stands from the outstanding overall impact of this power processing subsystem within a whole system in terms of volume/area, weight, and efficiency, being the power management the limiting factor in the portability and operating lifetime, particularly in wireless and mobile systems such as cellular phone terminals - especially those with increasing power demands, such as in third-generation (3G) systems. Other applications include microsystem supplies and circuits and systems for ubiquitous computing and communications. The ultimate step thus consists in the fully monolithic integration of the power converter together

with the same circuits which constitute its load within either the same substrate or chip package, yielding a complete Powered System on a Chip (PSOC).

The direct correlation between the increase in switching frequency and the reduced weight and volume of reactive energy-storing elements (or, in planar integrated processes, the occupied area) dictates a clear increase in switching frequency if miniaturization and eventually on-chip integration is targeted. Nevertheless, increasing the switching frequency directly increases several losses within different elements which compose the power converter topology, such as both wire and core losses in magnetic elements and switching losses in semiconductor switches. Previous attempts to integrate switching power converters, either on the same substrate or with a Multi-chip-module (MCM) approach, have focused on the technology implications of integrating the converter (with outstanding results of converters operating in 10-250MHz range, 0.2-5W range and efficiencies up to 56-80% [1-4]), but lack a proper-modeled analytical derivation of the converter key parameters such as operating frequency and inductor and capacitor value. This paper presents a modeling of the previous issues and provides an analytical framework for exploring the design space for future designs.

2 Analytical model for design space exploration

The modeling for design space exploration requires the selection of a topology over which that exploration is to be carried out. Accounting for battery-operated systems requirements as key target systems, and without loss of generality of the approach, in the rest of this work a boost topology is considered (see, e.g., the high-performance boost converter used to supply high-efficiency RF power amplifiers described in [5]).

The main idea is to analytically define a figure of merit trading the converter circuit DC-DC conversion functionality (through the output ripple Δv_o), its power processing functionality by means of its power efficiency η (through the evaluation of the different loss mechanisms) and the implementability in an integrated environment (through the occupied area). On the other hand, all these parameters depend on the three-dimensional design space given by inductor and capacitor values and switching frequency (L, C, f_s). In the following, an ordered derivation of these dependencies is provided. The *a priori* parameters and assumptions of this analysis are application-oriented such as the topology, the input and output voltage levels (V_{in}, V_o), the average supply current demand, as well as all the technology-related parameters.

2.1 Output voltage ripple

Consider the boost switching DC-DC converter topology suited to integrated environments shown in Fig. 1 (note the use of synchronous rectification by means of complementary operated transistors as well as a MOSFET-based capacitor).

Firstly, its output ripple is given by the relationship

$$\Delta v_o = \frac{V_o D T_s}{RC} = \frac{V_o D}{RC f_s} = f_{\Delta v_o}(L, C, f_s) \quad (1)$$

which requires to include the dependence of duty cycle on input and output voltages, taking into account DC winding losses in the inductor (modeled by means of R_w):

$$D = 1 - \frac{1 + \sqrt{1 - 4 \left(\frac{V_o}{V_{in}} \right)^2 \frac{R_w}{R}}}{2 \frac{V_o}{V_{in}}} \quad (2)$$

where the undefined symbols have their usual meaning [6].

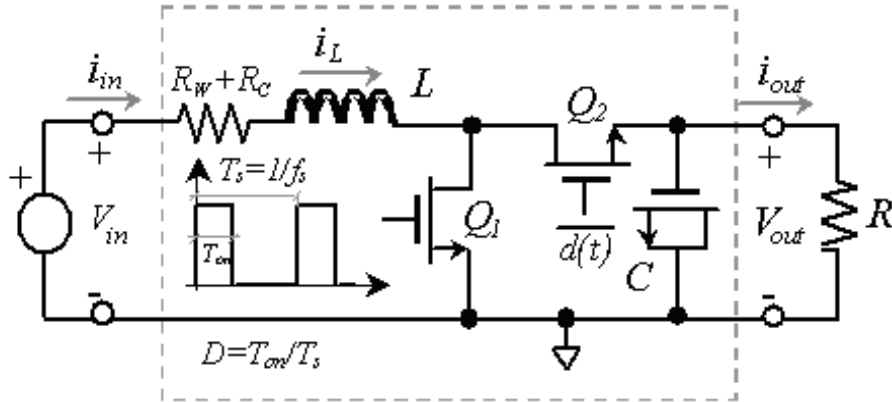


Figure 1: Boost switching power converter topology suited to IC implementation.

2.2 Efficiency

Secondly, the efficiency of the converter, which is the function involving more dependencies, is described by means of a first-order model that includes losses in the magnetic element (both static due to the winding resistance P_{L-DC} and frequency-dependent due to magnetic core losses P_{L-core}),

and losses in the semiconductor switching elements P_{Q-all} , both static and dynamic:

$$\eta = \frac{V_{in}I_L - P_{L-DC} - P_{L-core} - P_{Q-all}}{V_{in}I_L} = f_\eta(L, C, f_s) \quad (3)$$

where I_L stands for the inductor current *rms* value.

The DC losses due to the winding resistance are modeled by:

$$P_{L-DC} = I_L^2 R_w = \frac{2\rho}{A_w} \sqrt{\frac{\pi l_c}{\mu_c}} \left[\left(\frac{V_o}{RD'} \right)^2 \frac{1}{12} \left(\frac{V_{in}D}{Lf_s} \right)^2 \right] \sqrt{L} \quad (4)$$

where the squared inductor current, which is composed of the terms due to the switching transistors in a complementary operation, is given by:

$$I_L^2 = \left(\frac{V_o}{RD'} \right)^2 \frac{1}{12} \left(\frac{V_{in}D}{Lf_s} \right)^2 = I_{Q1}^2 + I_{Q2}^2. \quad (5)$$

As far as the magnetic core losses due to magnetic hysteresis are concerned, they can be modeled as being linearly dependent on frequency and quadratically dependent on the maximum inductor current [7]:

$$P_{L-core} = k_{core} f_s i_{Lmax}^2 + k_{core} f_s \left(\frac{V_o}{RD'} + \frac{V_{in}D}{2Lf_s} \right)^2. \quad (6)$$

Regarding the losses in switching elements, the DC term is due to the ON resistance of the transistors, which yields:

$$\begin{aligned} P_{QDC-all} &= P_{Q1DC} + P_{Q2DC} = R_{on} (I_{Q1}^2 + I_{Q2}^2) \\ &= \frac{L_g \nu_s}{\mu_n \left(\frac{V_o}{R} + \frac{DV_{in}}{2Lf_s} \right)} \left[\left(\frac{V_o}{RD'} \right)^2 \frac{1}{12} \left(\frac{V_{in}D}{Lf_s} \right)^2 \right] \end{aligned} \quad (7)$$

the width of the transistors designed following [4], this is, by avoiding carriers to reach saturation currents (which are accounted for through the saturation velocity v_s), is:

$$W_g = \frac{I_{Lmax}}{C_{ox} (V_{gson} - V_T) \nu_s} = \frac{\frac{V_o}{R} + \frac{DV_{in}}{2Lf_s}}{C_{ox} (V_{gson} - V_T) \nu_s} \quad (8)$$

and the ON resistance, in turn, is given by:

$$R_{on} = \frac{V_{DS}}{I_D} = \frac{L_g}{\mu_n C_{ox} W_g (V_{gson} - V_T)} = \frac{L_g \nu_s}{\mu_n \left(\frac{V_o}{R} + \frac{DV_{in}}{2Lf_s} \right)} \quad (9)$$

where the undefined symbols regarding MOS transistors have their usual meaning [8].

The switching losses in transistors are directly proportional to both the switching frequency and the rise (t_r) and fall (t_f) times:

$$P_{Qswitching-all} = P_{Q1switching} + P_{Q2switching} = P_{QDC-all} \frac{f_s}{2} (t_r + t_f). \quad (10)$$

Accounting for the capacitive load that the power transistors impose to their drivers [9]:

$$C_{in} = W_g L_g C_{ox} = \frac{L_g \left(\frac{V_o}{R} + \frac{DV_{in}}{2Lf_s} \right)}{(V_{gson} - V_T) \nu_s}, \quad (11)$$

the number of stages of tapered buffers in optimally designed drivers for the power transistors is given by:

$$N = \text{round} \left[\ln \left(\frac{C_{in}}{f a n_{in}} \right) \right] \quad (12)$$

so that, finally, the fall and rise times are given by:

$$t_r = t_f = t_{pd} \left[(N - 1) e + \frac{C_{in}}{f a n_{in} e^{N-1}} \right]. \quad (13)$$

From previous expressions (7) and (10), the total losses due to the transistors are given by:

$$\begin{aligned} P_{Q-all} &= P_{QDC-all} + P_{Qswitching-all} = P_{QDC-all} \left[1 + \frac{f_s}{2} (t_r + t_f) \right] \quad (14) \\ &= \frac{L_g \nu_s}{\mu_n \left(\frac{V_o}{R} + \frac{DV_{in}}{2Lf_s} \right)} \left[\left(\frac{V_o}{RD'} \right)^2 \frac{1}{12} \left(\frac{V_{in} D}{Lf_s} \right)^2 \right] \left[1 + \frac{f_s}{2} (t_r + t_f) \right]. \end{aligned}$$

2.3 Occupied area

Thirdly, the physical resources for the implementation of the converter, which, as opposite to the classical weight and volume indexes, in an integrated environment consist in the occupied area, correspond to:

$$Area = A_C + A_L + 2A_Q = f_A (L, C, f_s) \quad (15)$$

where the area occupied by the capacitor (implemented by the densest structure in a CMOS environment, which is a MOS-capacitor [10]), is given by:

$$A_C = C \frac{t_{ox}}{\epsilon_{ox}}. \quad (16)$$

The area due to the inductor is dependent on the technology and implementation method (see [1-3,11-17]), but can be generally described by a certain inductive density (δ_L):

$$A_L = \frac{L}{\delta_L} \quad (17)$$

and the area of each transistor is directly given by its dimensions, considering the length of each transistor to be minimum, so as to save area, improve current drive and reduce R_{ON} , and accounting for expression (8):

$$A_L = W_g L_g = \frac{\frac{V_o}{R} + \frac{DV_{in}}{2Lf_s}}{C_{ox} (V_{gson} - V_T) \nu_s} L_g. \quad (18)$$

2.4 Figure of merit

Finally, all the previous dependencies are collected in a single figure of merit, which depends on the three design parameters and allows the design optimization. Starting from the definition of a generic figure of merit with both proportional (β) and exponential (γ) weights:

$$\Gamma(x_1, \dots, x_n) = \frac{\prod_i \beta_i f_i^{\gamma_i}(x_1, \dots, x_n)}{\prod_j \beta_j f_j^{\gamma_j}(x_1, \dots, x_n)}. \quad (19)$$

the following figure of merit is proposed for the design space to be explored:

$$\Gamma(L, C, f_s) = \frac{f_\eta(L, C, f_s)}{f_A^2(L, C, f_s) f_{\Delta v_o}(L, C, f_s)}. \quad (20)$$

Note that the area dependence is square-weighted so as to solve the ill-conditioned solution of $\Delta v_o \rightarrow 0$ while $A \rightarrow \infty$, which corresponds to infinite area capacitors yielding zero ripple.

To illustrate the representation of this three-dimensional figure of merit function, Fig. 2 depicts an example of all three functions (η , Δv_o , A) as three bidimensional cuts, this is, with a family of two-input surfaces parametrically varied by the third parameter.

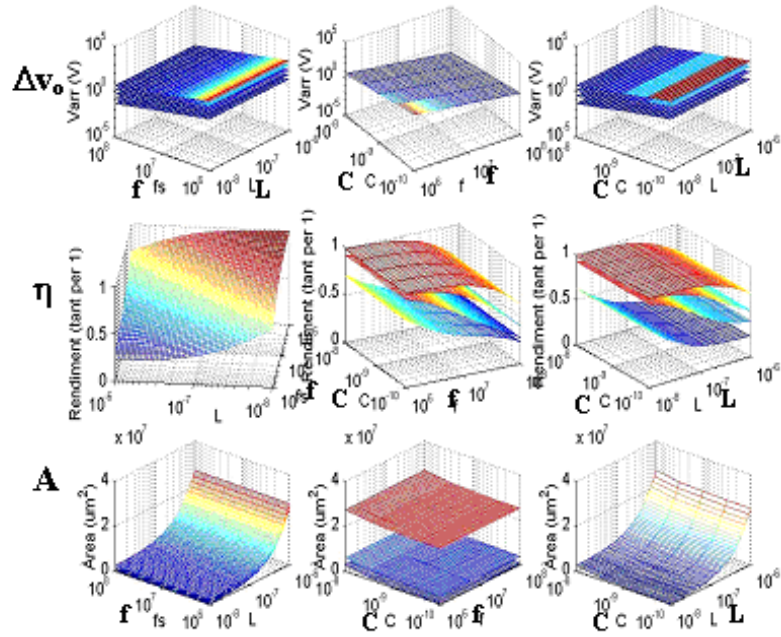


Figure 2: Design space exploration. From top to bottom: output ripple, efficiency, and occupied area ($k_{core} = 0$ case), $f_s = \{1 \text{ MHz}, 100 \text{ MHz}\}$, $L = \{10 \text{ nH}, 1 \mu\text{H}\}$, $C = \{100 \text{ pF}, 10 \text{ nF}\}$.

Fig. 3 (a) shows the three representative functions (1), (3), (15) for the case in which, apart from their previously presented modeling, two inequalities are included so as to impose design restrictions. The considered restrictions are the maximum allowed ripple ($\Delta v_o < \Delta v_{o_max}$), which depends on the load circuit specification, and the maximum allowable current through transistors ($i_Q < i_{max}$), which is included to reflect specifications on stress and reliability issues.

In Fig. 3, two important behaviors are observed. On the one side, compared to Fig. 2, the inclusion of core losses (k_{core}) results in local maxima for the efficiency, as expected regarding both inductor value and switching frequency design input variables. On the other side, the addition of design inequalities superimposed to the functions restricts possible solution design points over the design space, as it is better illustrated in the projections shown in Fig. 3(b).

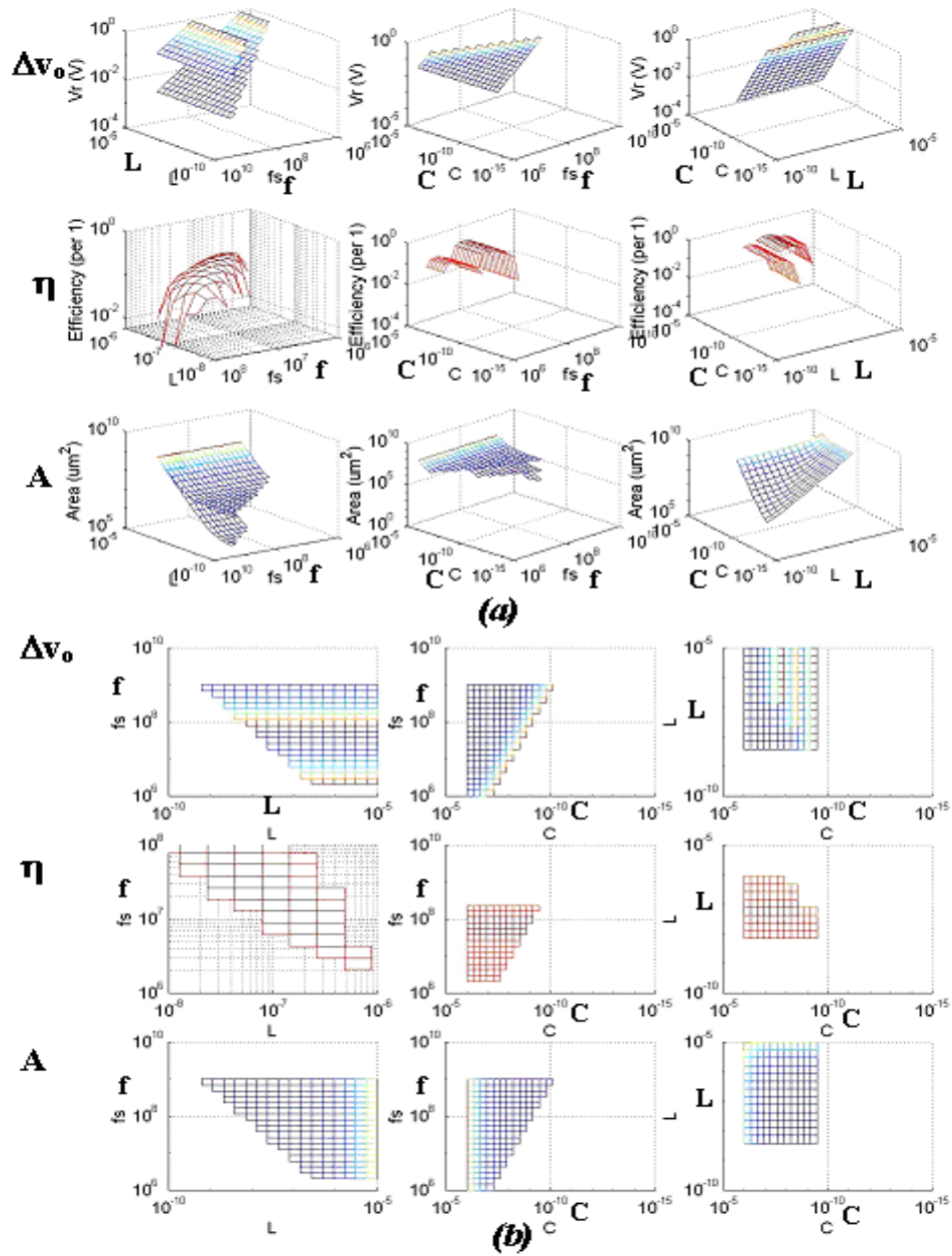


Figure 3: (a) Design space exploration for $\Delta v_{o_max} = 1$ V, $i_{max} = 1$ A; (b) projection over design input variables, $f_s = \{1$ MHz, 10 GHz $\}$, $L = \{100$ pH, 10 μ H $\}$, $C = \{1$ fF, 10 μ F $\}$.

3 Design space exploration for a particular micro-electronic technology

As a particular target case, the previous generic framework has been studied with particular parameters from a standard $0.35\mu\text{m}$ CMOS technology.

Retaining the views and axes definition from Fig. 3 representation, Fig. 4 shows two design space explorations by varying both the maximum allowed ripple Δv_{o_max} and the maximum allowable current through transistors i_{max} . It is interesting to note that, for some cases, local figure of merit singular points are obtained, whether in other cases the restrictions impose figure of merit maxima within the function domain frontier.

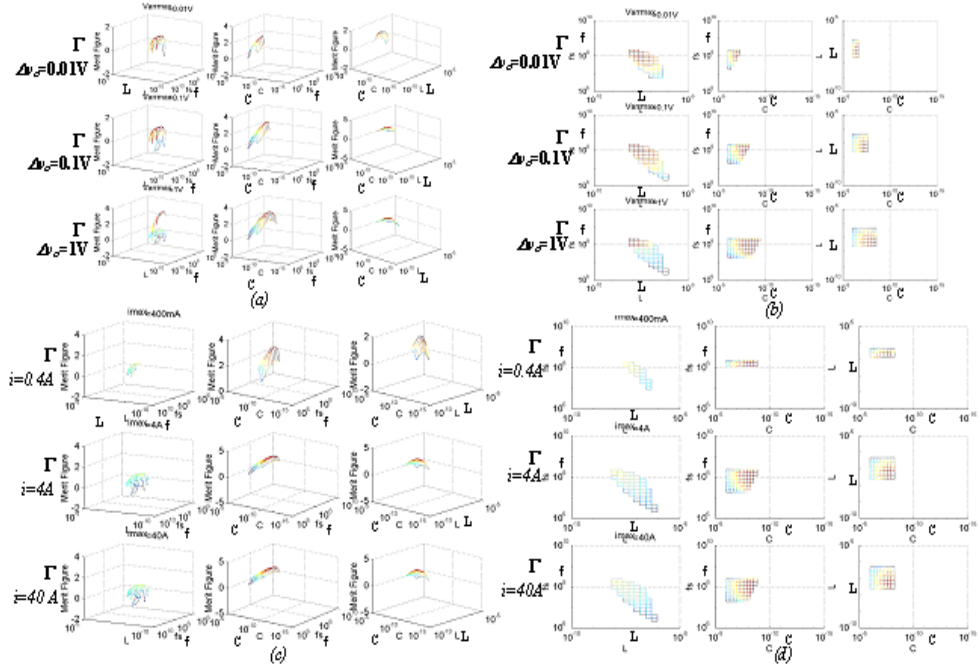


Figure 4: Design space exploration (a) and (b) output ripple constraint variation $\Delta v_{o_max} = [0.01\text{ V}, 0.1\text{ V}, 0.01\text{ V}]$; (c) and (d) maximum inductor current constraint variation $i_{max} = [0.4\text{ A}, 4\text{ A}, 40\text{ A}]$, $f_s = \{1\text{ MHz}, 10\text{ GHz}\}$, $L = \{100\text{ pH}, 10\ \mu\text{H}\}$, $C = \{1\text{ fF}, 10\ \mu\text{F}\}$.

4 Simulation results for a high frequency boost DC-DC power converter

Results from Fig. 4 for the $\Delta v_{o_max} = 0.1V$ and $i_{max} = 0.4A$ case provide an optimum figure of merit design parameters yielding the integrable converter of Fig. 5(a). For this $f_s = 100MHz$ and $L = 30nH$ boost converter, Fig. 5(b) shows full transistor-level simulation results of the output voltage, validating the functionality of the design.

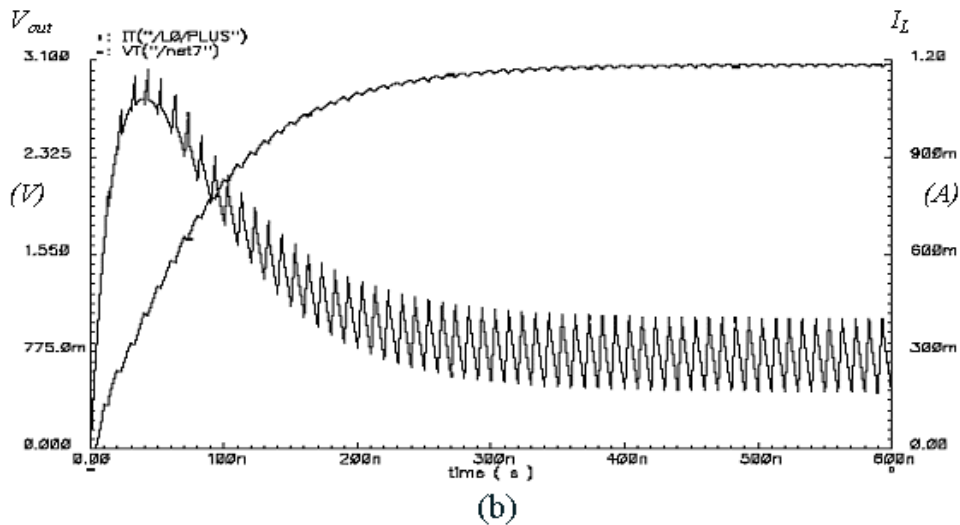
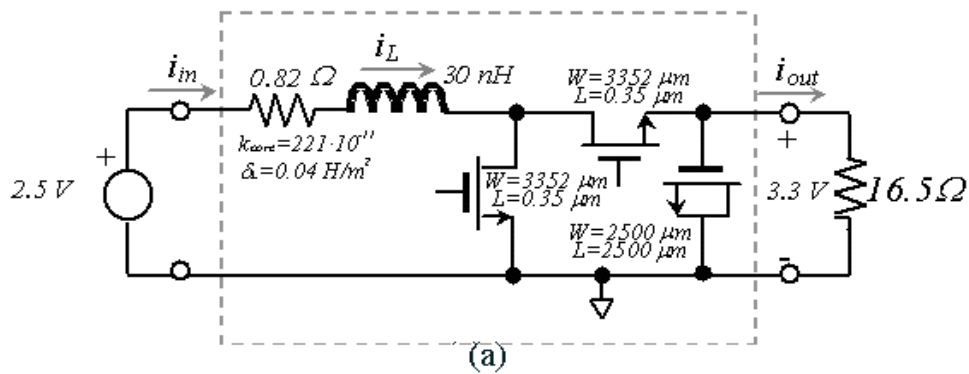


Figure 5: (a) Integrated high frequency boost converter prototype; (b) Output voltage and inductor current simulation results for 100 MHz switching frequency.

5 Conclusions

This work describes the research on an analytical framework for design space exploration pursuing the full on-chip integration of switching power converters. Particular results for a standard $0.35\mu\text{m}$ CMOS technology have revealed the existence of design singular points, which have been validated through simulation results for a high frequency boost converter prototype suited to integration. On-going work includes the refinement of the modeling from technological aspects while maintaining the optimization framework. Future work also includes the analytical derivation of design parameters by means of the geometric programming nonlinear optimization technique [18].

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