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High power factor forward AC-DC converter with low storage capacitor voltage stress

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Abstract

Forward converters generally exhibit poor power factor when employing in the AC-DC conversion, due to the presence of zero input current near the zero crossing of line input voltage. In this paper, a single-switch forward converter with high power factor and low storage capacitor voltage stress is proposed. By adding a stack up voltage on top of the reflected input voltage on the forward converter secondary, the dead angle of input current is eliminated. The storage capacitor voltage is also kept smaller than the peak input voltage throughout entire line and load conditions. Power factor correction and fast output regulation are achieved simultaneously by using only a single switch and a single voltage-feedback control loop. Parameters that affect the storage capacitor voltage and input current are examined. Experimental results showed the effectiveness of the proposed converter.

1 Introduction

Owing to the increasing concern about the harmonic distortion in line input current drawn by switch-mode power converters, power factor correction (PFC) techniques have been employed in the design of off-line power converters in order to comply with international standards such as IEC 1000-3-2 specifications. Among numerous PFC circuits developed to achieve power

factor close to unity, the boost converter is the most popular topology due to its simple circuitry and low cost. For applications, especially for low power applications, that requires transformer isolation or stepping down voltage, flyback converters are commonly used due to their simple configuration and low component count.

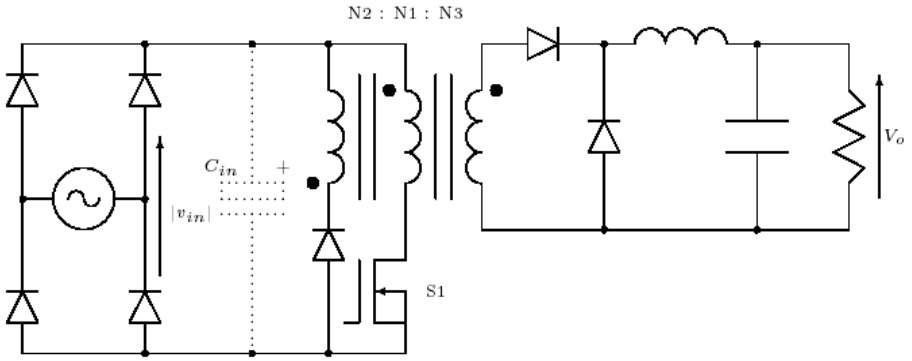

Figure 1: Forward converter serves as a power factor correction circuit.

Forward converter has the advantage of lower peak output current and less leakage energy related problems than those of a flyback converter. However, a normal forward converter, as shown in Fig. 1 (without the input capacitor C_{in}), is unable to use in AC-DC conversion because the bridge diode blocks the current path for the reset winding during the turn-off period of power switch S1. Moreover, energy transfer to output ceases during the interval when the rectified input voltage $|v_{in}|$ is lower than the reflected output voltage on primary (i.e. V_o*N1/N3), resulting in distorted input current. Even with C_{in} inserted for transformer reset, the input current will be very much distorted since no input current can flow into the circuit when the input voltage is lower than the voltage on C_{in}. By placing the reset winding on the transformer secondary, the aforementioned problems are solved [1]. Apart from providing a reset path for the converter (transferring reset energy to the output capacitor), the reset winding also serves as a flyback converter when $|v_{in}|$ is lower than V_o*N1/N3 and thus eliminates the dead angle of input current. However, the converter output contains substantial ripple voltage at line frequency. To remove this ripple voltage, [2, 3] attempted to inject an anti-phase ripple voltage into the output with the same magnitude and frequency. This is done by using another capacitor, which stores the energy from reset winding, and an auxiliary switch

with a sophisticated control system to provide this feature. But it is not a cost-effective solution for low-power applications.

Single stage PFC converters (SSPFC), which are formed by integrating the PFC circuit with a DC-DC regulator circuit, aimed at reducing the cost and simplifying the power stages and control of the converter [4-12]. By solely controlling the change of output, power input (with PFC) from line and regulation of output voltage can be done concurrently by sharing the same switch(es). Examples of circuits that combine a boost PFC converter and a forward DC-DC regulator have been proposed in [7-9]. Instead of acquiring energy from the line, the forward regulator stage takes energy from the intermediate storage capacitor which has relatively constant voltage. The boost PFC stage can achieve high power factor when the inductor runs in discontinuous conduction mode (DCM) and the duty cycle of power switch keeps roughly constant. The main drawback of SSPFC is the high voltage stress on the intermediate storage capacitor due to lacking control of its voltage. The paper [9] proposed to add a DC voltage above the rectified input voltage so that the dead angle of input current of the forward converter is removed. Nevertheless, the converter still suffered from high voltage stress on the storage capacitor due to the presence of boost inductor. As a result, semiconductor devices, such as transistors and diodes with high voltage rating, should be used. This also limits the practical use of SSPFC in wide input voltage applications. Recently, direct power transfer concept has been introduced in which an extra winding is inserted in parallel with the output and coupled to the boost inductor [10-12]. A portion of input energy stored in the boost inductor will be diverted to the output directly through this coupled winding. The voltage stress, as well as the voltage swing on the storage capacitor when line and load varies, are both reduced. However, the storage capacitor voltage cannot drop below the peak line input voltage due to the stepping up of input voltage by the boost inductor.

In this paper, a new high power factor single-switch forward AC-DC converter (SSFC) with low storage capacitor voltage is presented. To eliminate the dead angle of input current, a stack up voltage source is introduced on top of the reflected input voltage on transformer secondary during the turn-on period of power switch. In this way the input power can still transfer to output (i.e., charging up the output inductor) even when the reflected rectified input voltage on secondary is lower than the output voltage. In [9], the DC voltage added above the rectified input voltage is used to charge up the boost inductor. All the energy stored in the boost inductor will be diverted to the storage capacitor. Therefore the storage capacitor voltage is high and cannot drop below the peak input voltage. For the proposed SSFC, the

stack up voltage plus the reflected input voltage are used to charge up the output inductor directly. The storage capacitor is fed by the reset energy of transformer, which is much smaller compared to that of a boost inductor. Due to the absence of boost inductor placing at the front-end of the proposed circuit, the voltage on the intermediate storage capacitor keeps relatively low.

The proposed SSFC with the stack up voltage source has the following features:

- the input current has no dead angle, thereby improving the power factor;
- voltage stress on the storage capacitor is reduced and can drop below the peak input voltage, permitting the use of smaller storage capacitor and lower voltage rating semiconductor devices;
- power factor correction and fast output voltage regulation are done by only a single switch and a single loop controller.

In Section 2, the operation principle and modes of the proposed SSFC will be described. In Section 3, the steady state analysis will be carried out to derive the expressions of duty ratio and storage capacitor voltage. The analysis of input current will be depicted in Section 4. With the design example given in Section 5, the experimental demonstrations to verify the proposed concept will be given in Section 6 and followed by the conclusions in Section 7.

2 Proposed circuit and its operation

2.1 Operation principle

The proposed SSFC is shown in Fig. 2. It consists of a normal forward converter (with transformer T1, power switch S1, output diodes D_3 and D_4, and output inductor L_o), two additional diodes D_2 and D_5, and an auxiliary transformer T2, which is used to implement the stack up square-wave voltage source. The primary side of T2 with diode D_2 is connected across the intermediate storage capacitor C_B and the power switch S1; the secondary winding of T2 is connected in series with L_o. Capacitor C_B functions not only as an intermediate storage element for the SSFC but also the stack up voltage source. The reset energy from T1 and T2 are both delivered to C_B through D_1 and D_5, respectively, when S1 turns off. The

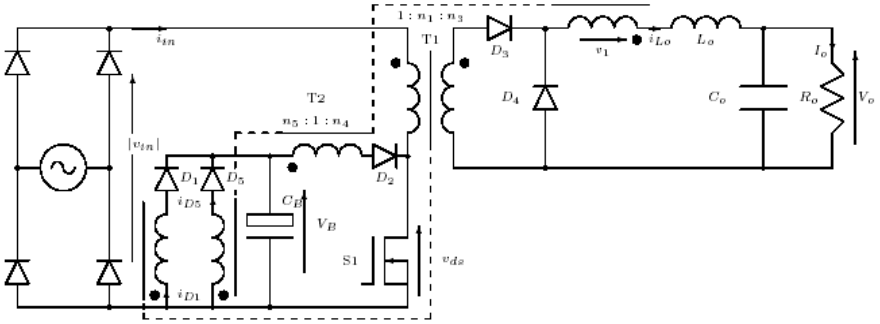

Figure 2: Proposed Single-Switch Forward AC-DC PFC Converter (SSFC).

output power is controlled by sensing the output voltage to a compensation network and adjusting the duty ratio of S1 using conventional pulse with modulation (PWM). Power factor correction is automatically achieved by DCM operation of both transformers T1 and T2.

Fig. 3a shows the conceptual diagram of the proposed method. It is a simplified diagram showing the output side of the proposed SSFC. The converter with transformer T1 is modeled as a square-wave voltage source v_s and another square-wave voltage source v_1, which is derived from C_B and used to stack up v_s, is placed in series with L_o. When the power switch turns on (in Fig.3b), v_s becomes $n_3|v_{in}|$ and v_1 equals $n_4 V_B$. The voltage across the output inductor L_o is $(n_3|v_{in}|+n_4 V_B - V_o)$ and it charges up linearly. Even if $|v_{in}|$ reaches zero, L_o can be charged up by setting v_1 slightly higher than V_o. Therefore, input current can flow into the circuit once $|v_{in}|$ rises from zero and the dead angle of input current is eliminated. When the power switch turns off (in Fig. 3c), v_s goes negative and D_3 is reverse biased. v_1 also becomes negative and equals $V_B(n_4/n_5)$. The voltage applied across L_o is $(V_B(n_4/n_5) + V_o)$ and it is discharged through D_4.

Fig. 4 shows the effect of the proposed stack up voltage method at the time when S1 is turned on. Without the stack up voltage (i.e. $v_1 = 0$), there is a dead angle of input current, which is expressed as θ_1, during the line period where no input current can flow because $n_3|v_{in}| < V_o$ and diode D_3 is reverse biased. If v_1 is added, the dead angle of input current decreases to θ_2. When $v_1 = V_o$, it is expected that the dead angle will be completely eliminated so that input current can flow all the time once $|v_{in}|$ rises from zero.

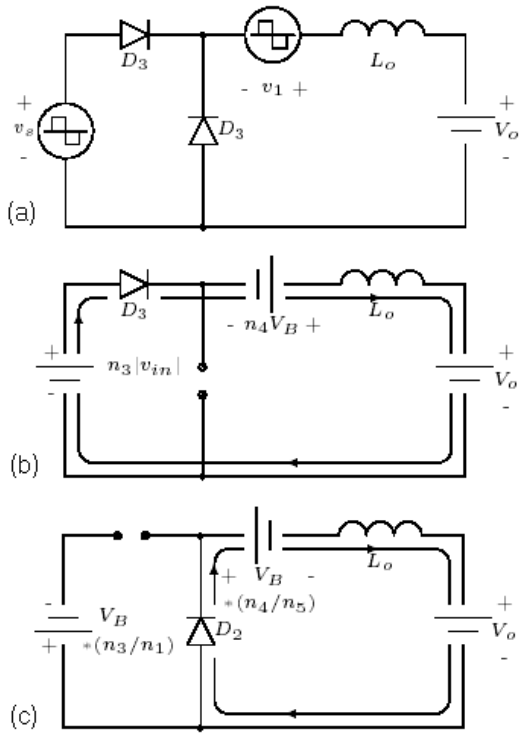

Figure 3: Conceptual diagram of the proposed method: (a) conceptual diagram; (b) when power switch turns on; (c) when power switch turns off.

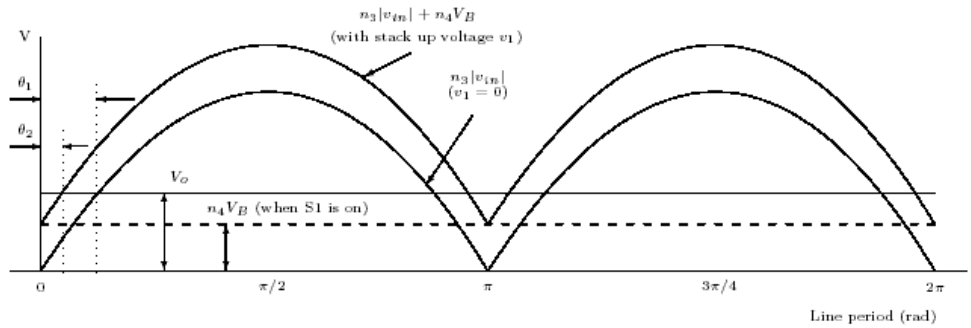

Figure 4: Conceptual diagram of the stack up voltage method at the time S1 is turned on.

2.2 Operation modes

To facilitate the steady state analysis, parasitic components of the power switch and diodes are ignored. Assuming the coupling between both transformer windings to be perfect, the magnetizing inductance of T1 and T2 are modeled as L_{M1} and L_{M2}, respectively. Theoretical switching waveforms of proposed SSFC is illustrated in Fig. 5. By inspection of the circuit, there are four modes of operation. The circuit operation is fully analyzed as follows.

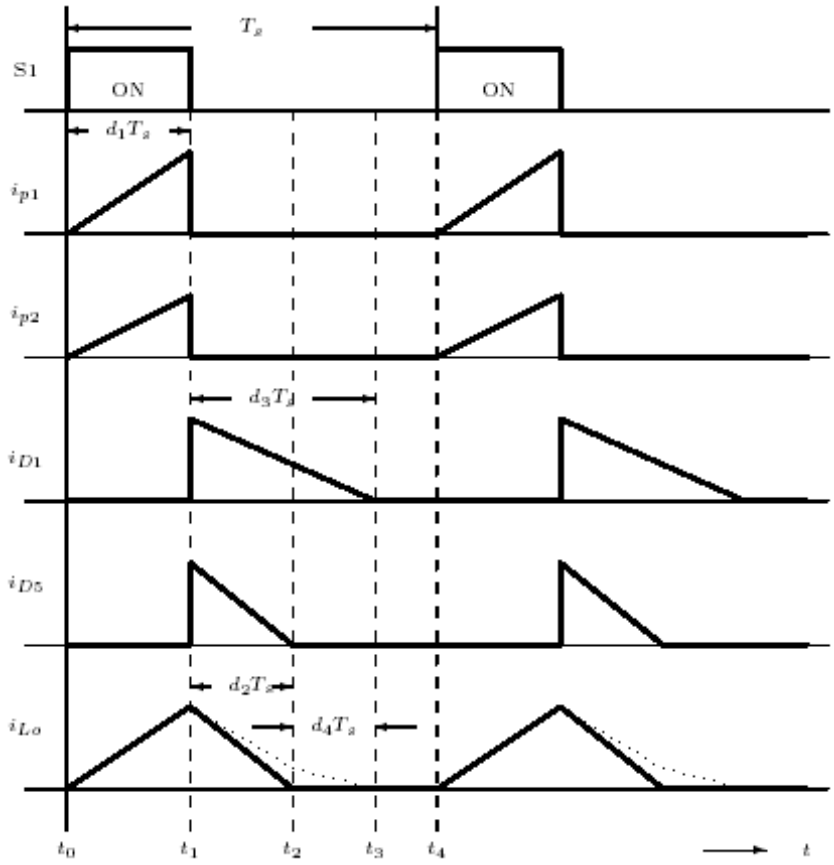

Figure 5: Key switching waveforms of the proposed SSFC.

Mode 1 ($t_0 - t_1$) [Fig. 6a]: Switch S1 is turned on, power is transferred from both voltage sources, rectified input voltage $|v_{in}|$ through T1 and storage capacitor C_B through T2, to the load. D_4 is reverse biased but D_3 enters

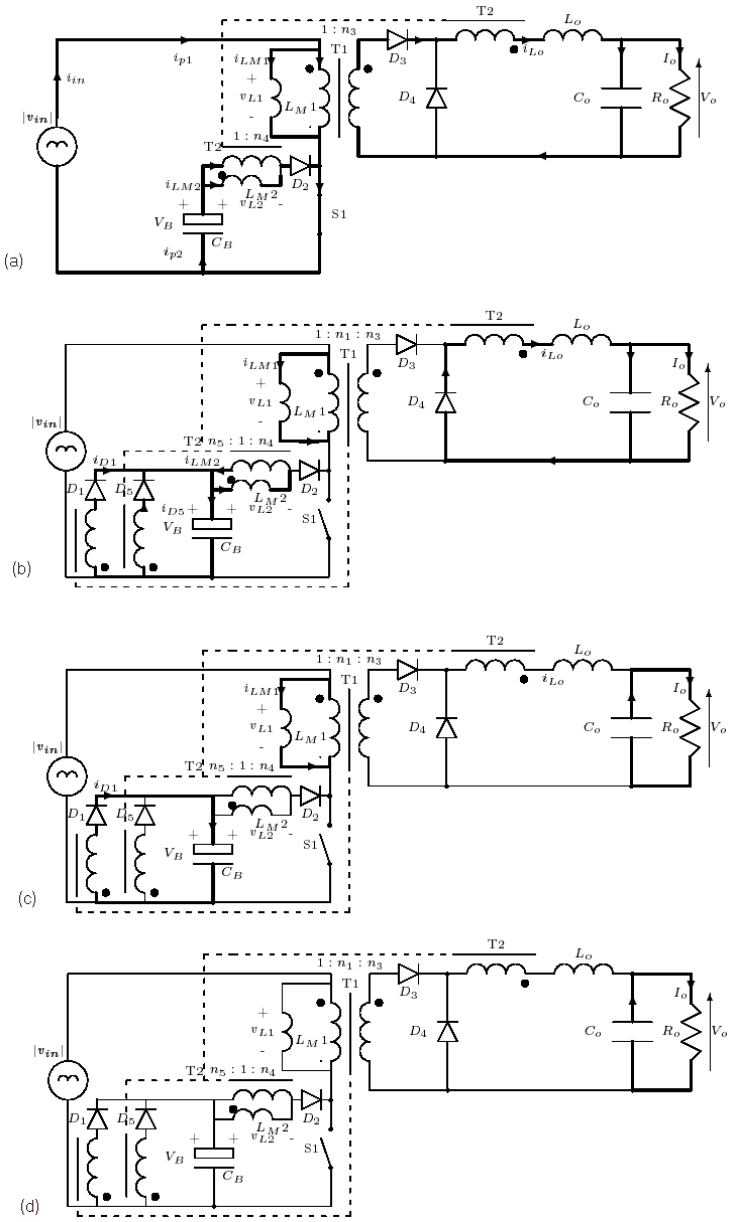

Figure 6: Operation mode diagrams of SSFC: (a) mode 1; (b) mode 2; (c) mode 3; (d) mode 4.

conduction state. The output inductor L_o is being charged up linearly with a rate

$$\frac{di_{Lo}}{dt} = \frac{n_3|v_{in}| + n_4 V_B - V_o}{L_o}. \tag{1}$$

As the dotted ends of the reset windings are positive with respect to the non-dotted end, diodes D_1 and D_5 are reverse biased. Let the mutual inductance between primary and secondary (not the reset winding in series with D_1) sides of T1 be M_{T1}, under perfect coupling it becomes

$$M_{T1} = n_3 L_{M1}. \tag{2}$$

The voltage applied across magnetizing inductance L_{M1} is $|v_{in}|$. From Ampere's law, the input current is

$$i_{p1} = i_{LM1} + n_3 i_{Lo}. \tag{3}$$

Substituting (1) and (2) into (3) and differentiating both sides, we get the rate of change of i_{p1}

$$\frac{di_{p1}}{dt} = \frac{|v_{in}|}{L_{M1}} + n_3 \frac{n_3|v_{in}| + n_4 V_B - V_o}{L_o}. \tag{4}$$

The voltage applied across magnetizing inductance L_{M2} is V_B. Using the same method as above, the rate of change of i_{p2} is given by

$$\frac{di_{p2}}{dt} = \frac{V_B}{L_{M2}} + n_4 \frac{n_3|v_{in}| + n_4 V_B - V_o}{L_o}. \tag{5}$$

Mode 2 ($t_1 - t_2$) [Fig. 6b]: Mode 2 is initiated by turning off S1. The voltage applied on the non-dotted end (which is positive with respect to the dotted end) of T1 secondary equals $V_B(n_1/n_3)$ and D_3 is reverse biased. Since i_{Lo} cannot sustain a sudden change in its direction, D_4 is forward biased and i_{Lo} continues to flow with a downslope equals

$$\frac{di_{Lo}}{dt} = \frac{-(n_4 V_B + n_5 V_o)}{n_5 L_o}. \tag{6}$$

Meanwhile, the non-dotted ends of both reset windings are changed to positive with respect to dotted ends and both equal V_B. D_1 and D_5 are in conduction state. The reset energy from both T1 (through D_1) and T2 (through D_5) are coupled to C_B. The rate of change of i_{D1} is written as

$$\frac{di_{D1}}{dt} = \frac{-V_B}{n_1^2 L_{M1}}. \tag{7}$$

Since i_{Lo} passes through the secondary winding of T2, the voltage applied across its reset winding, which is clamped to V_B, can also be written as

$$V_B = M_{T2}\frac{di_{Lo}}{dt} - n_5^2 L_{M2}\frac{di_{D5}}{dt} \tag{8}$$

where M_{T2} is the mutual inductance between secondary and reset windings of T2 and is equal to $n_4 n_5 L_{M2}$. Substitution of (6) into (8), the rate of change of i_{D5} is given by

$$\frac{di_{D5}}{dt} = \frac{-1}{n_5^2 L_{M2}}\left(V_B + n_4 L_{M2}\frac{n_4 V_B + n_5 V_o}{L_o}\right). \tag{9}$$

Mode 3 ($t_2 - t_3$) [Fig. 6c]: After i_{D5} reaches zero, mode 3 begins. During this mode, all energy in T2 is released. The current i_{Lo} may reach zero at time t_2, otherwise i_{Lo} will continue to discharge (follows the dotted line of i_{Lo} in Fig. 5) with a rate equals

$$\frac{di_{Lo}}{dt} = \frac{-V_o}{n_4^2 L_{M2} + L_o}. \tag{10}$$

The reset current in T1 continues to flow through D_1 to store in C_B. The output capacitor C_o sustains the output voltage. This mode ends when i_{D1} falls to zero.

Mode 4 ($t_3 - t_4$) [Fig. 6d]: In this mode, C_o continues to deliver power to the load. All the reset energy of T1 is completely transferred to C_B. The next switching cycle begins when S1 is turned on again. If i_{D1} has not yet reached zero at t_4 when S1 turns on again, T1 will be run in CCM. A sudden rise in i_{Lp1} will happen and cause distortion in the input current. But it can be prevented by proper selection of circuit parameters, to be depicted in Section 3.

3 Steady state analysis

The storage capacitor voltage V_B greatly affects the voltage ratings of semiconductor devices such as transistor and diodes. Additionally, V_B determines the stack up voltage which will help eliminate the dead angle of input current. In this section, steady state analysis for the proposed SSFC will be carried out to derive the relationship between the ratio of storage capacitor voltage to peak input voltage, M_2, and the circuit parameters such as the turns ratios (n_3, n_4 and n_5) and magnetizing inductances of T1 and T2 (L_{M1} and L_{M2}), the output inductor L_o and the output voltage V_o. With

these circuit parameters, the equation of input current will also be formed. For the purpose of this analysis and design, the duty ratio expression of S1 will be obtained first.

3.1 Duty ratio of power switch S1

Referring to Fig. 5, the turn-on time ratio of S1 is defined as d_1 and the discharge time ratio of T1, i_{D1}, is d_2. Using the voltage-second balance condition on L_{M2}, the time ratio d_2 can be expressed by

$$d_2 = n_5 d_1. \tag{11}$$

Similarly, by calculating the voltage-second balance condition on L_o, the time ratio d_4 is obtained:

$$d_4 = \frac{L_o}{n_4^2 L_{M2} + L_o} \frac{n_3|v_{in}| - (n_5+1)V_o}{V_o} d_1. \tag{12}$$

As $|v_{in}|$ varies from ground to its peak value during the line period, d_4 derived in (12) may go beyond zero, which is impossible in reality. Indeed, d_4 is equal to zero when $|v_{in}| \leq (n_5+1)V_o/n_3$, that is equivalent to the time i_{Lo} reaches zero at t_2 as shown in Fig. 5. The average output inductor current $\bar{i}_{Lo}$ at each switching period T_s also forms different shapes according to (12).

Case 1: $|v_{in}| \leq (n_5+1)V_o/n_3$: Under this condition, d_4 equals zero. When S1 turns on, the current in L_o rises from t_0 to its peak

$$i_{Lo,pk} = \frac{n_3|v_{in}| + n_4 V_B - V_o}{L_o} d_1 Ts. \tag{13}$$

After S1 turns off at t_1, i_{Lo} falls back to zero at t_2. Combining (1) and (11), $\bar{i}_{Lo}$ is given by

$$\bar{i}_{Lo} = \frac{(n_3|v_{in}| + n_4 V_B - V_o)(n_5+1)}{2L_o} d_1^2 T_s. \tag{14}$$

Considering the output equation, we have

$$I_o = \frac{V_o}{R_o}. \tag{15}$$

Since the average output current I_o is equal to $\bar{i}_{Lo}$, substituting (15) into (14) gives the duty ratio of S1

$$d_1 = \sqrt{\frac{2L_o}{R_o T_s} \frac{V_o}{(n_5+1)(n_3|v_{in}| + n_4 V_B - V_o)}}. \tag{16}$$

Case 2: $|v_{in}| > (n_5 + 1)V_o/n_3$: In this case, i_{Lo} continues to discharge during the period of d_4Ts, and d_4 obeys (12). The peak value of i_{Lo} at t_2 equals

$$i_{Lo,pk} = \frac{V_o}{n_4^2 L_o} d_3 Ts. \tag{17}$$

By inspecting the waveform of i_{Lo} and using (15), the duty ratio of S1 is given by

$$d_1 = \sqrt{\frac{2L_o}{R_o T_s} \frac{L_o V_o^2}{L_o V_o a_1 + a_2}} \tag{18}$$

where

$$a_1 = n_3(1 + 2n_5)|v_{in}| + n_4(1 + n_5)V_B - [1 + n_5(2 + n_5)]V_o,$$
$$a_2 = (n_4^2 L_{M2} + L_o)[n_3|v_{in}| - (n_5 + 1)V_o]^2.$$

Note that the duty ratio d_1 in both cases is dependent on the load resistance R_o and the rectified input voltage $|v_{in}|$. When the load drops (i.e., R_o increases) or the input voltage increases, d_1 is decreased. In addition, d_1 is not a constant throughout the line period, it falls to minimum at peak input voltage, and vice versa. Fig. 7 shows an example of d_1 for half of line period.

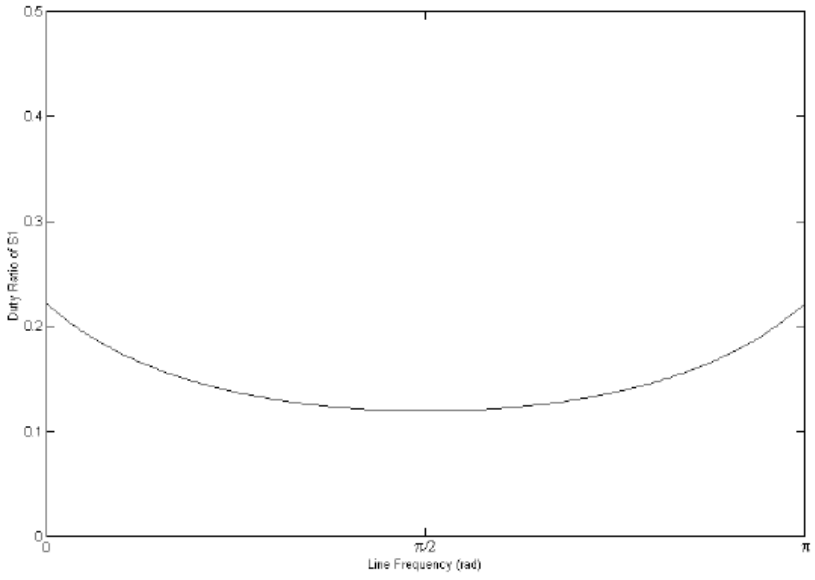

Figure 7: Example of duty ratio of S1, d_1.

3.2 Expression of storage capacitor voltage

During the interval of S1 turn-on, charge is taken away from C_B through T2 to the load. The average discharging current of C_B, which equals the average charging current $\overline{i}_{Lp2}$ at period $t_0 - t_1$, is given by

$$\begin{aligned} \overline{i}_{discharge} &= \overline{i}_{Lp2} \\ &= \frac{d_1^2 T_s}{2L_{M2}L_o}\left[n_3 n_4 L_{M2} V_m|\sin\theta| + (L_o + n_4^2 L_{M2})V_B - n_3 n_4 L_{M2} V_o\right] \end{aligned} \tag{19}$$

where $|v_{in}| = V_m|sin\theta|$. V_m is the peak input voltage and θ is the angular frequency of line voltage expressed in radians. For the period when S1 is turned off, the reset energies from T1 and T2 will be both stored in C_B. Using the voltage-second balance condition on L_{M1}, the discharge time ratio, d_3, of T1 through D_1 is expressed as

$$d_3 = n_1 d_1 \frac{V_m|\sin\theta|}{V_B}. \tag{20}$$

Substitution of (20) into (5) gives the average diode current:

$$\overline{i}_{D1} = \frac{d_1^2 T_s}{2L_{M1}} \frac{(V_m|\sin\theta|)^2}{V_B}. \tag{21}$$

The average diode current i_{D5} can be found by combining (9) and (11) is written as

$$\overline{i}_{D5} = \frac{d_1^2 T_s}{2L_{M2}L_o}\left[(n_4^2 L_{M2} + L_o)V_B + n_4 n_5 L_{M2} V_o\right]. \tag{22}$$

In the steady state, the average storage capacitor current over a half line period should be zero, therefore

$$\int_0^\pi \overline{i}_{Lp2} d\theta - \left(\int_0^\pi \overline{i}_{D1} d\theta + \int_0^\pi \overline{i}_{D5} d\theta\right) = 0. \tag{23}$$

Defining the ratio of output voltage to peak input voltage as

$$M_1 = \frac{V_o}{V_m} \tag{24}$$

and substituting (19), (21), (22) and (24) into (23), we obtain a transcendental expression of M_2:

$$M_2 = \frac{V_B}{V_m} = \frac{G_1(\theta)}{G_2(\theta) - G_3(\theta)} \tag{25}$$

where

$$G_1(\theta) = \int_0^{\pi} \frac{d_1^2 |\sin\theta|^2}{L_{M1}} d\theta, \tag{26}$$

$$G_2(\theta) = \int_0^{\pi} \frac{d_1^2 \left[n_3 n_4 L_{M2} |\sin\theta| + (L_o + n_4^2 L_{M2}) M_2 - n_4 L_{M2} M_1 \right]}{L_{M2} L_o} d\theta, \tag{27}$$

$$G_3(\theta) = \int_0^{\pi} \frac{d_1^2 \left[(n_4^2 L_{M2} + L_o) M_2 + n_4 n_5 L_{M2} M_1 \right]}{L_{M2} L_o} d\theta. \tag{28}$$

Note that for the proposed SSFC, M_2 is independent of the load R_o. While there is no straightforward analytical solution to this integral, it can be solved numerically for specific cases.

4 Analysis of input current

Consider the current i_{L1} in Fig. 5, the area of i_{L1} divided by a switching period T_s is the instantaneous average input current, which is given by

$$\bar{i}_{in} = \frac{d_1^2 T_s V_m}{2 L_{M1} L_o} \left[(L_o + n_3^2 L_{M1}) |\sin\theta| + n_3 L_{M1} (n_4 M_2 - M_1) \right]. \tag{29}$$

It can be seen from (29) that the condition to eliminate the dead angle of input current is achieved when

$$n_4 M_2 \geq M_1. \tag{30}$$

Case 1: $n_4 M_2 = M_1$: In this case, the input current becomes

$$\bar{i}_{in} = \frac{d_1^2 T_s V_m (L_o + n_3^2 L_{M1})}{2 L_{M1} L_o} |\sin\theta|. \tag{31}$$

Equation (31) shows that the proposed SSFC is capable of obtaining sinusoidal current that follows the rectified input voltage if d_1 is a constant throughout the line cycle. In fact, d_1 is the primary variable that affects the shape of input current. As shown in Fig. 7, d_1 is time-varying and reaches its lowest point when the rectified input voltage reaches its peak value. Depending on the curvature of d_1, which is measured from its peak value at $|v_{in}|$=0 down to its lowest point, the average input current may therefore have a flatted-top current shape or even a valley-shape if the curvature of d_1 is deeper. This will increase the third harmonic component (and also

other higher odd harmonic components but with decreasing magnitude) to the input current and deteriorate the power factor.

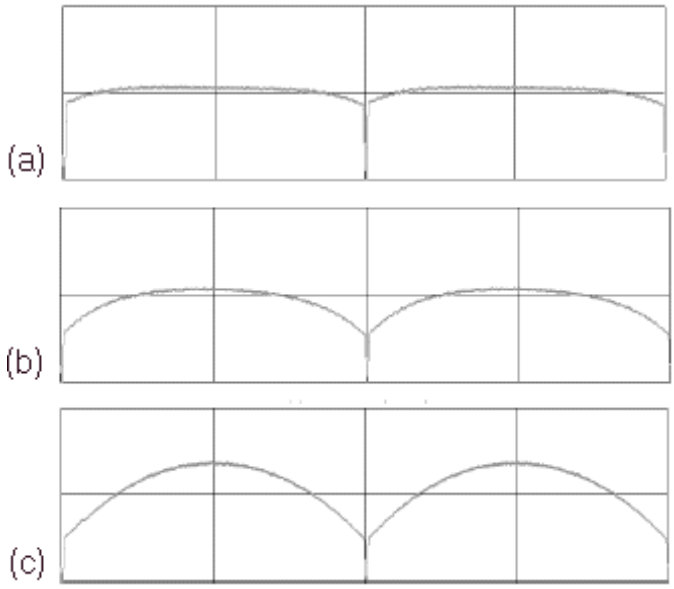

Figure 8: Simulated input current (i_{in}) waveforms of SSFC with different values of n_3 and L_o: (a) $n_3 = 0.5$; $L_o = 30\mu$H; (b) $n_3 = 0.3$; $L_o = 30\mu$H; (c) $n_3 = 0.3$; $L_o = 100\mu$H.

Case 2: $n_4 M_2 > M_1$: Under this condition, L_o will be charged up by the storage capacitor even when input voltage reaches zero. Therefore input current can still flow into the circuit and a step of input current will occur at the zero crossing of input voltage. The instantaneous average input current at this moment is

$$\bar{i}_{in} = \frac{d_1^2 T_s V_m}{2L_o} \left[n_3 (n_4 M_2 - M_1) \right]. \tag{32}$$

On the one hand, the step of input current helps to improve the power factor if the shape of input current is not sinusoidal. For most single-stage PFC converters, which merged the boost converter with other transformer isolated DC-DC converter, the input current is of a bell-shape [4-12]. This is due to the non-linear property of boost converter applying in input current shaping. But it was experimentally verified in [6] that the step of input current, which is introduced by the regenerative clamping capacitor, improves the power

factor. It is due to the fact that the step current reinforces the fundamental component of input current, though it also adds to odd harmonics of input current with smaller quantity. On the other hand, as the proposed SSFC inherits unity power factor capability, the step of input current should be as small as possible but adequate to remove the dead angle of input current.

To improve the power factor of proposed SSFC, d_1 should be maintained close to a constant (i.e. a straight line) over the line cycle. The sine term in (16) and (18) is the component to produce the curvature property of d_1. If n_3 is decreased, the effect of the sine term will be diminished. At the same time, it can be seen from (29) that when n_3 is reduced, the step of input current near the zero crossing of input voltage is also reduced. However, to eliminate the dead angle of input current for the entire line condition, a small input current step is needed. In the meantime, the sine term in (29) should be magnified so that the input current drawn by the SSFC can be close to pure sinusoidal. This is done by increasing L_o. To confirm the discussion above, Fig. 8 shows a series of simulated input current waveforms of the SSPFC by PSpice with different values of n_3 and L_o. The harmonic components of input current under different cases are also investigated and shown in Fig. 9.

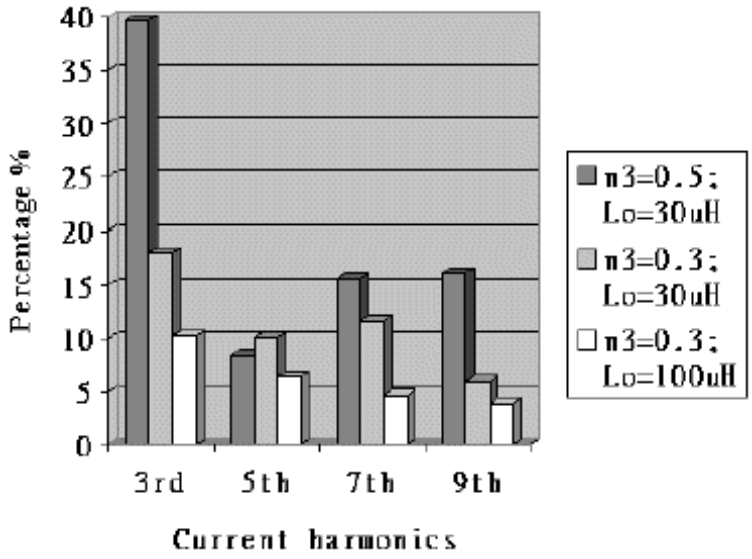

Figure 9: Input currents harmonics of SSFC with different values of n_3 and L_o.

5 Simplified design example of the proposed SSFC

Since the experimental demonstration is just to verify the proposed concept and analysis, a simplified design of the proposed SSFC with 50W/28V DC output and 90V_{rms} input is described. Constant switching frequency of 100kHz is chosen. To confirm the preceding analysis, two series of experimental setup are carried out with different values of n_3.

Now, the turns ratio n_1 is considered. As mentioned in the operation mode analysis, if transformer T1 is not completely reset before the turn-on instant of S1, the input current will be distorted. More important, if the change in flux density during the turn-on period of S1 is not equal to the return change during the off period, the core will be saturated. In order to shape the input current closely sinusoidal and prevent core saturation, i_{D1} must reach zero before the next switching cycle and the following inequality must be satisfied

$$d_3 \leq 1 - d_1. \tag{33}$$

The worst case for i_{D1} to stay in DCM is at full load and minimum line conditions where the input voltage reaches its peak (i.e. $\sin\theta = 1$). In this case, duty ratio of S1 reaches the critical value $d_{1,crit}$. It is because the boundary of DCM and CCM of T1 starts at the peak input voltage and CCM of T1 spreads wider from this point if the load is further increased. Substitution of (33) into (20), gives the inequality

$$n_1 \leq \frac{1 - d_{1,crit}}{d_{1,crit}} M_2. \tag{34}$$

Therefore the turns ratio of transformer T1, n_1, must be smaller than the above equation for the entire line and load conditions.

By assuming $L_{M1} = 370\mu$H, $L_{M2} = 1230\mu$H, $n_4 = n_5$=0.55, and $L_o = 30\mu$H and referring to (25), $M_2 = 0.536$ for $n_3 = 0.3$ and $M_2 = 0.544$ for $n_3 = 0.4$. The critical duty ratio $d_{1,crit}$, which happens at full load and peak input voltage, for both cases can be determined either by (16) or (18). Using the above circuit parameters, $(n_5 + 1)V_o/V_m = 0.34$. This indicates that with $n_3 = 0.3$, (16) is used while for $n_3 = 0.4$, (18) is used. Therefore, the critical duty ratio for $n_3 = 0.3$ and 0.4 are 0.62 and 0.58, respectively. To maintain T1 in DCM, the maximum turns ratio n_1 should be calculated. Moreover, for a fair comparison, n_1 should be the same for both setup. Substituting the values of M_2 and $d_{1,crit}$ of the two setup into (34), we have $n_1 \leq 0.32$ for n_3=0.3 and $n_1 \leq 0.39$ for n_3=0.4. In this prototype, $n_1 = 0.3$ is selected.

6 Experimental verifications

In order to verify the operation and performance of the proposed SSFC, a 50-W/28-V DC with input voltage of 90V$_{rms}$ hardware prototype was implemented and tested. The following components were used for implementation of the circuit: C_B - 220μF; D_1, D_2 and D_5 - MUR460; D_3 and D_4 - MUR860; S1 - MTW14N50E; C_o - 3300μF; T1 - ETD34 core with 11 primary turns, 4 (5) secondary turns for $n_3 = 0.3$ (n_3=0.4) and 4 reset turn; T2 - ETD34 core with 20 primary turns, 11 secondary turns and 11 reset turns. The proposed circuit employs RCD snubbers across both transformers to absorb the leakage energy, as well as to reduce the voltage spike induced on the drain-to-source voltage of S1.

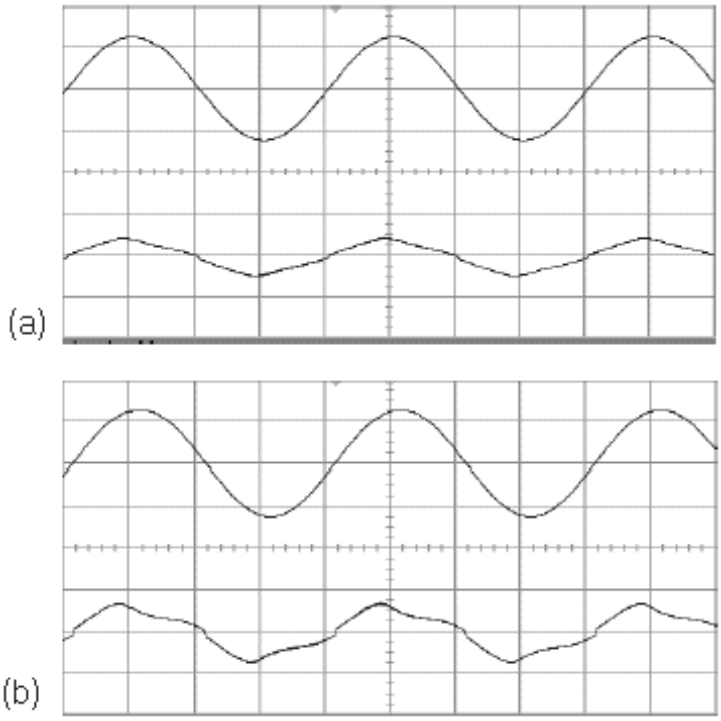

Figure 10: Measured line voltage (v_{in}) and current (i_{in}) waveforms of SSFC with different values of n_3. (a) $n_3 = 0.3$; upper trace: v_{in} 100V/div; bottom trace: i_{in} 200mA/div; time base: 5 ms/div; (b) $n_3 = 0.4$; upper trace: v_{in} 100V/div; bottom trace: i_{in} 200mA/div; time base: 5 ms/div.

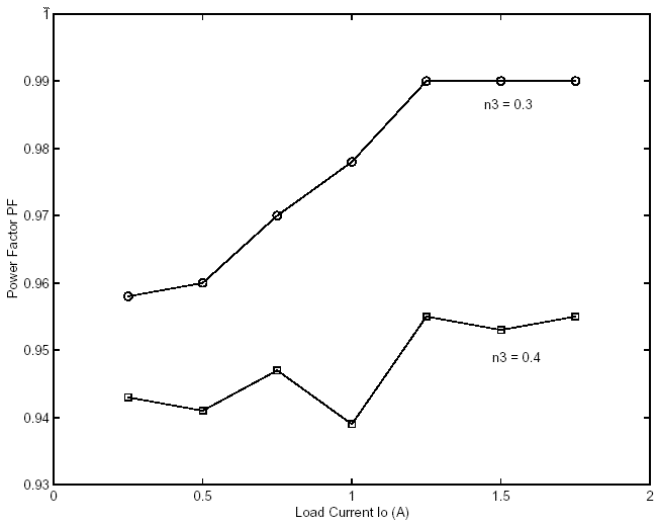

Figure 11: Measured power factor with different values of n_3.

Figs. 10a and 10b show the typical line voltage and current waveforms of the experimental SSFC for $n_3 = 0.3$ and $n_3 = 0.4$, respectively. These figures show that the proposed converter does not contain the dead angle of input current. Fig. 11 illustrates the power factor of both implementations for entire load range and that agrees the analysis of power factor improvement with smaller n_3. It is interesting to note from Fig. 12 that the storage capacitor voltage V_B is much lower than the peak input voltage. For the existing single-stage PFC converters, power factor is improved at the expense of increasing the storage capacitor voltage due to the presence of boost inductor. However, it can be observed that, for the proposed SSFC, one can find a proper value of n_3 which improves the power factor without changing V_B. This feature is particularly desirable for wide line input applications. The experimental V_B is a bit smaller than the calculated values because in the analysis it is assumed in lossless condition and the coupling of transformers is perfect. But it is already a good approximation to predict V_B. Fig. 13 shows that the storage capacitor voltage is kept low throughout the line variations.

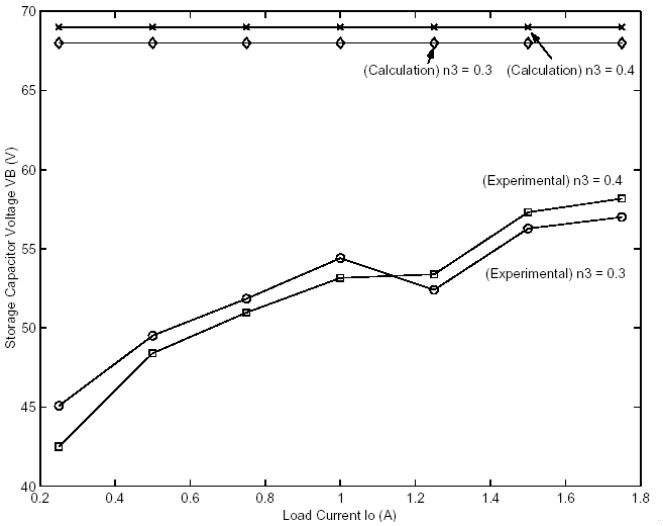

Figure 12: Calculated and measured storage capacitor voltage with different values of n_3.

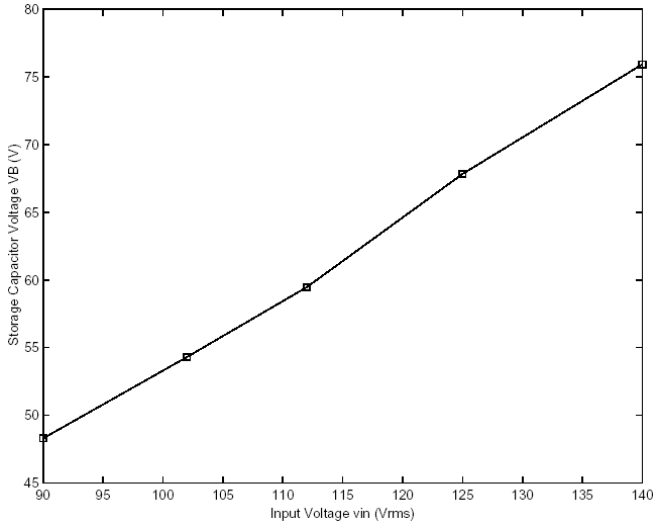

Figure 13: Measured storage capacitor voltage with line variations.

7 Conclusions

This paper presented a novel single-switch forward power-factor-corrected AC/DC converter operating in DCM. By eliminating the dead angle of line current, the proposed converter exhibited high power factor. Moreover, due to the absence of boost inductor (as being inserted in existing single-stage converter for shaping the input current), which steps up the storage capacitor, the proposed circuit possessed low voltage stress on the storage capacitor. This voltage can even reach below the peak input voltage throughout the entire line and load variations. Therefore, smaller storage capacitor and semiconductors such as diodes and main switch can be used for wide input applications. With few components added, it is expected that the proposed circuit is also suitable for compact power supply with power factor correction.

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