HAIT Journal of Science and Engineering B, Volume 2, Issues 5-6, pp. 848-868

Design and realisation of integrated inductor with low DC-resistance value for integrated power applications

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Received 1 March 2005, accepted 17 August 2005

Abstract

This paper presents a new topology of inductor allowing a decrease of the conductor serial resistance. After validating the concept of conductors interleaving, technological process flow and results are presented.

1 Introduction

The integration of various components of a static converter is actually the principal stake in the field of Power Electronics. Indeed, considering the development of distributed architectures or "Systems-On-Chip", new techniques must be developed to reduce size and reach better efficiencies [1]. Even if much progress have been done in this field, some technological obstacles still prevent reaching powerful supply in a smaller place. The main resolved subjects are focused on semiconductors, which allow by their switching a power transfer control [2]. Indeed, these active components are more and more efficient to convert the energy with low losses in switching or conduction mode, and their control is very easy with simple, low consumption and cheap command circuits. Moreover, the switching frequency increase

(from 75kHz to 1MHz) has allowed an important size reduction of converters.

The last problem to achieve the complete integration of converters, which present powers lower than 100W, consists in integration of passive elements, especially inductors [3]. They are actually compos of an electric conductor on a magnetic support mounted on a metallic board. These technologies must be replaced by more compact solutions. Indeed, even if these elements present good efficiency, their size limits their behaviour at high frequency. Besides, they actually define the converter size [4].

Many technological solutions devoted to the integration of passive elements, can be found in the literature. They propose to improve the integration density by decrease of losses and higher operating frequencies [5-7]. The size of components can be reduced by using the surface or volume micromachining techniques, in order to realize the inductor on silicon wafers. But few inductors are actually available as many technological problems occur. Therefore, the actual existing inductors are designed for their high switching operation frequencies rather than their storage capabilities. After an overview of the different integrated inductors existing solutions, we present the one chosen by LAAS-CNRS and its study the influence of geometrical and shape parameters on inductance and resistance values.

The approach based on reduction of the conductor's width and space implies an increase in DC resistance. Therefore, those structures do not support a high current density and present higher Joule losses. As the aim of our work consists in realizing an inductive structure with high inductance and low electrical resistance value, we present in the third part an original solution for DC resistance reduction, based on an optimization of the inductor topology by the use of interleaved conductors. The structure is actually composed of n wires coiled up and short-circuited at each extremity. The section of the equivalent conductor is therefore increased n-fold. As a consequence, DC resistance is reduced. After a theoretical study of wire parallelization and a comparison with electromagnetic simulations obtained with an FEM tool, Coventoware, we will evaluate the effect of parallelization on the global inductance and resistance values. A comparison between single and parallelized conductor performances will be discussed. At last, the electrical results coming from the characterization will be compared to simulation results. Conclusions will be drawn on the effectiveness of this original inductive structure.

2 Inductance design

2.1 Geometrical considerations

Three types of geometries are used to realise integrated inductors: solenoid, meander-type or spiral. The first one corresponds to a transposition of the discrete realization of inductor, where the wire winds around a magnetic core. But those three-dimensional realizations are not easily transposable with very small dimensions using microsystem technologies. Nevertheless, some solutions have been presented in the literature, as shown in Fig. 1 [8].

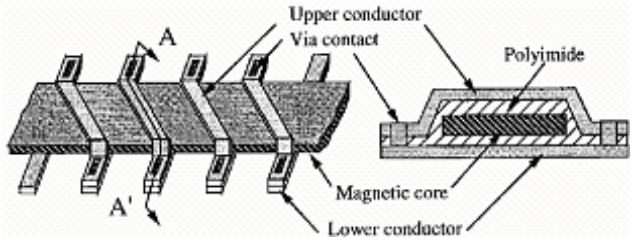


Figure 1: Solenoid integrated inductor [8].

Fig. 2 presents a meander-type inductance, which is based on alternating magnetic components and core places, where the magnetic material is winded round the conductor [9]. This method changes the obtained effects.

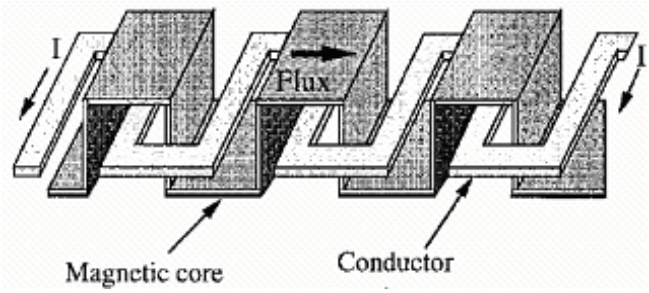


Figure 2: Meander-type integrated inductor [9].

Fig. 3 presents the integration method allowing the obtaining of a planar structure, which can be easily realized in a few technological steps. Most of the integrated inductors in the literature use spiral geometry [10,11]. They

can be realized on an insulating or magnetic substrate, or between two magnetic materials. They present the advantage of an easy technological realization as the main steps are done with surface micromachining. But, due to the spiral geometry, the magnetic flux can be divided into two components, parallel and perpendicular to the wafer surface. Therefore, it is difficult to integrate those types of structure, as the magnetic tore must cross the substrate surface to increase the efficiency of the structure.

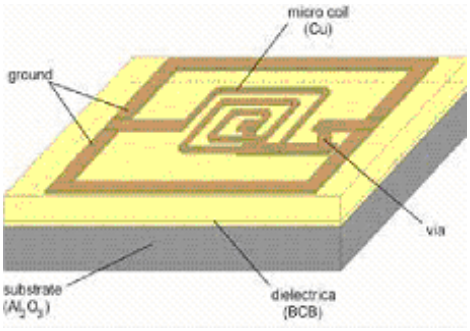


Figure 3: Spiral integrated inductor [1].

In the case of energy storage applications, two factors limit the amelioration of spiral inductances performances. On the one hand, a metallic deposition must be added to the magnetic circuit in order to decrease the magnetic reluctance. On the other hand, the inductance must present the higher quality factor Q (*i.e., the lowest possible resistance*), to reduce conduction losses. Below we focus our purpose on this type of inductance.

2.2 Mathematical evaluation

The main goal of the mathematical evaluation consists in an evaluation of the inductance value as a function of inductor and wire dimensions. There exist different shapes of planar inductor shown in Fig. 4. Afterwards, we focus our study on rectangular spiral conductors, placed on an insulated or magnetic substrate, as shown in Fig. 3. As a first mathematical evaluation, the inductance value of the planar inductor L_T can be determined by summing not only elementary self-inductances of each straight segment, but also mutual inductances:

$$L_T = L_0 + \sum M \tag{1}$$

where L_0 is the sum of elementary self-inductances and ΣM is the sum of all

mutual inductances. In our case, only mutual inductances linked to straight parallel conductor segments exist [12]. Moreover, in case of classical electronic circuits, negative mutual inductances are usually neglected compared to the global inductance.

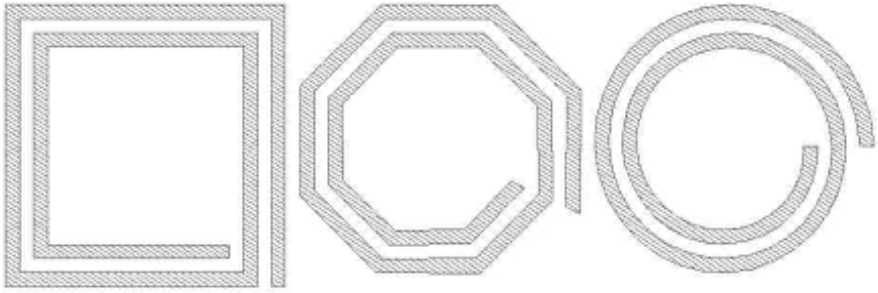


Figure 4: On-chip inductors realization: square, octagonal, and circular inductors.

In the literature, several mathematical methods exist to evaluate the inductance value, such as the Bereza, Bryan, Grover, or Terman methods. Depending on the mathematical method used, the influence of different geometrical parameters on inductance calculation differs. To evaluate it more precisely, a study was conducted to determine the inductance value using different methods [13]. The total inductance L_T is equal to the sum of positive and negative mutual inductances:

$$L_T = L_0 + M_+ - M_- \tag{2}$$

where M_+ is the sum of positive mutual inductances and M_- is the sum of negative ones. The mutual inductance M between two parallel conductors is a geometrical function of length l:

$$M = 2lQ \tag{3}$$

where Q is the mutual inductance parameter. The self-inductance value for a straight conductor with the magnetic permeability equal to 1, is given by

$$L = 2l_x.\left\{\ln\left[\frac{2l_x}{w+t}\right] + .50049 + \frac{w+t}{3l_x}\right\} \tag{4}$$

where L_x represent the segment inductance (*in nanohenries*), l_x, w, and t are, respectively, the segment length, width, and thickness (*in centimeters*).

Considering a single-turn square planar coil, we obtain:

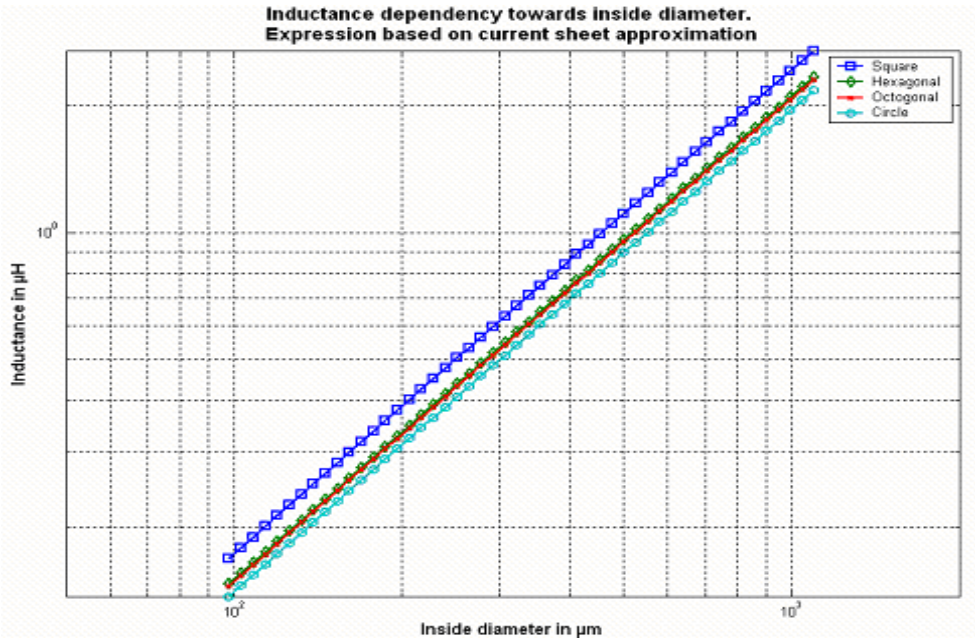
$$L_0 = \sum_{i=1}^{4} L_i. \tag{5}$$

In this case, only currents in parallel legs in opposite directions exist. Then, the positive mutual inductance in this coil vanishes:

$$M_+ = 0. \tag{6}$$

At last, negative mutual inductance is the sum of $M_{1,3}$, $M_{3,1}$, $M_{2,4}$, and $M_{4,2}$. As $M_{1,3}$ is the same as $M_{3,1}$ and similarly $M_{2,4}$ and $M_{4,2}$, then

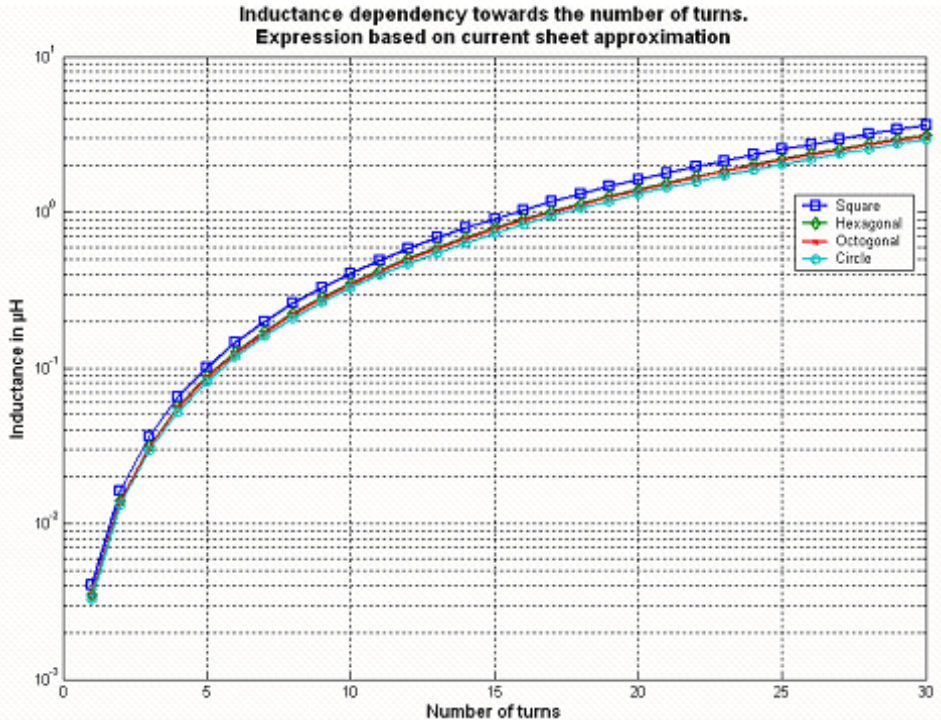
$$M_- = 2\left(M_{1,3} + M_{2,4}\right). \tag{7}$$



Graphic 1. Inductance dependence on the inside diameter.
$w = s = 1\mu$m; $t = 3\mu$m; $n = 20$.

Graphics 1 and 2 show, respectively, the inductance dependence on the inside diameter and number of turns for different shapes of inductors: square, hexagonal, octogonal, and circular. We used the value of width w

and space s equal to 1μm and the value of thickness t equal to 3μm. In Graphic 1, number of turns n is equal to 20; in Graphic 2, the outer diameter d_{out} is equal to 700μm. Independent of the parameters, the inductance topology giving the biggest inductance value is the spiral one.

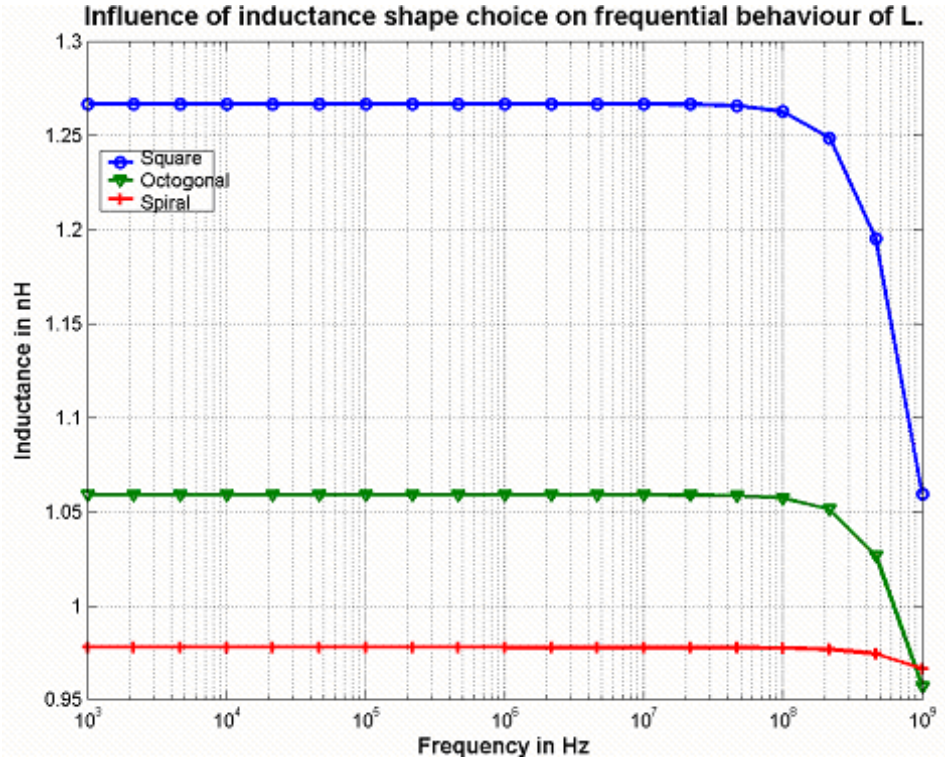


Graphic 2. Inductance dependence on the number of turns.
$w = s = 1\mu$m; $t = 3\mu$m; $d_{out} = 700\mu$m.

There are two major difficulties that must be overcome in order to improve the usefulness of this geometry. First, closed magnetic circuits must be completed using a thick magnetic material with high permeability to reduce magnetic reluctance and to minimize magnetic field interferences (*making the adhesion of the thick magnetic layer a concern*). Second, the spiral conductor must have the resistance as small as possible to reduce power consumption in the conductors.

2.3 Inductance evaluation with FEM model

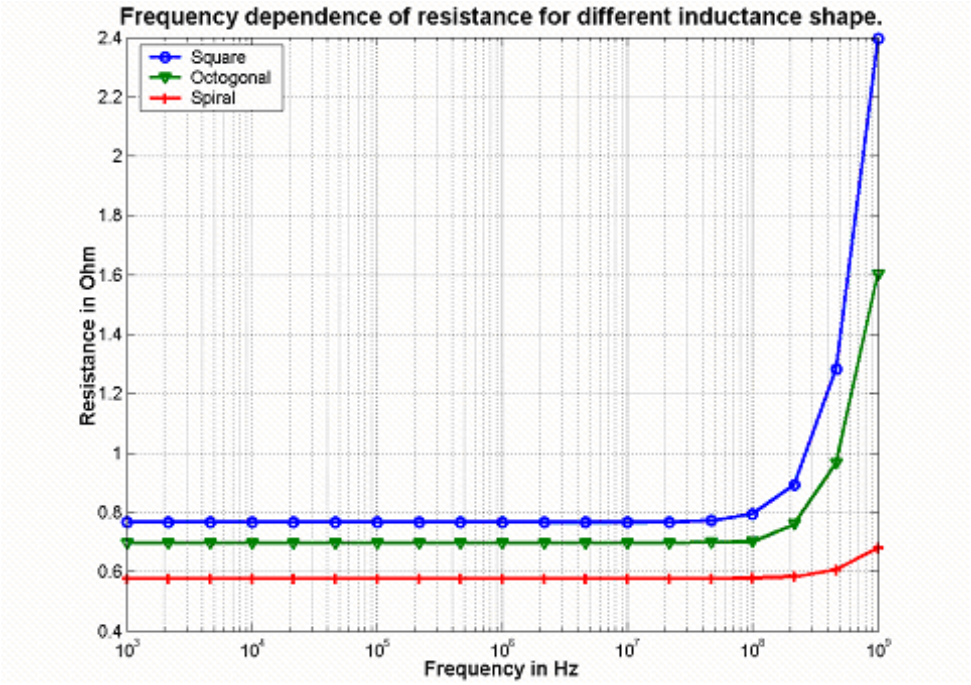
A very accurate numerical solution may be obtained by using a three dimensional finite element simulator. We chose to use the MemHenry module of Coventor solution [14,15]. It computes the frequency-dependent resistance, and inductance matrices for a set of conductors. This accurate, three-dimensional computation can be applied to magnetic sensor design, on-chip passive inductor analysis and parasitic extraction for packaging analysis. The module also builds Spice and Saber models, which can be configured to capture frequency-dependent skin and proximity effects.



Graphic 3. Frequency dependence of the inductance for different geometrical shape. $w = s = 1\mu$m; $t = 3\mu$m; $n = 20$.

MemHenry uses an integral equation approach that requires a mesh only in the interior of conductors, thus eliminating the need for the user to mesh all of free space. Combining this approach with a multipole-accelerated solution algorithm, MemHenry can complete the extraction of resistance and

inductance for complicated 3D structures rapidly. Using the same model, one can analyze the dependence of inductance with varying position, dimension, or even mechanical deformation.



Graphic 4. Frequency dependence of the resistance for different geometrical shape. $w = s = 1\mu$m; $t = 3\mu$m; $d_{out} = 700\mu$m.

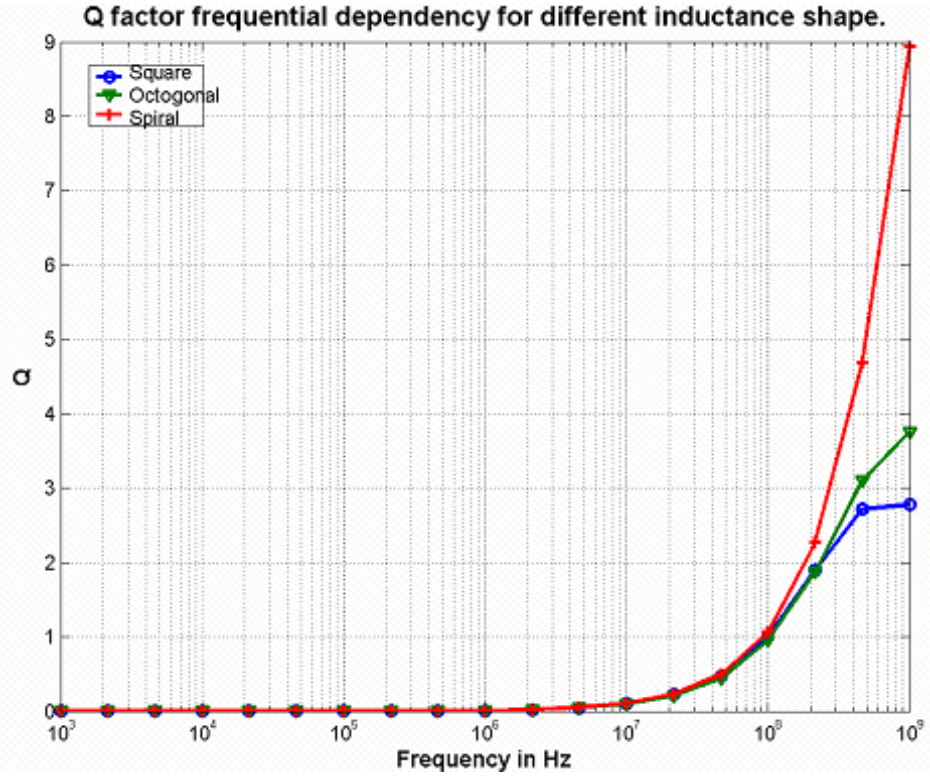
Our first task has been to validate the MemHenry module. For that, we have conducted several simulations to obtain the frequency dependence of inductance and resistance. Graphics 3 and 4 show this results for three different sample geometries. An important figure of merit for inductors is the quality factor Q, which can be estimated by [16]:

$$Q = \frac{Im\left[y_{11}\right]}{Re\left[y_{11}\right]} = \frac{L\omega}{R} \tag{8}$$

where L, R and ω are the inductance, resistance, and radiance frequency, respectively. Quality factors of inductors measured by this way increase linearly with frequency, reach a peak, and then decrease. This decrease is attributed to a capacitive coupling of signals through a parasitic metal to

substrate capacitor, C_{p1}. In general, this Q-estimation technique is valid for frequencies below the frequency corresponding to the peak value of Q. If the frequency is increased sufficiently, $\dfrac{Im\,[y_{11}]}{Re\,[y_{11}]}$ becomes zero. This point is the frequency at which the average magnetic energy storage is approximately equal to the average electric energy storage, or the self resonant frequency of the inductor.

Graphic 5 shows the frequency dependence of the Q-factor for different inductance shapes. It can be easily shown that the best values of Q are realized for a spiral shape. A straight-forward way to increase Q-factors is to reduce series resistance by thickening or widening conductors, although widening increases the parasitic capacitance to the substrate. This increase can limit the operating frequency range for the inductors. Therefore, we decide to limit thickness and try to realize interleaved conductors.



Graphic 5. Frequency dependence of Q-factor for different inductance shape. $w = s = 1\mu$m; $t = 3\mu$m; $d_{out} = 700\mu$m.

3 Interleaved conductors theory

3.1 Objectives

Different geometrical parameters of inductor directly influence the inductance and resistance values, in the case of inductor integration using planar technology: conductor width, spacing and thickness, inductor external diameter and number of turns. Previous work has demonstrated that conductors' thickness increasing does not influence the inductance value and significantly reduces the electrical resistance. But the inductor conception is limited by the conductor's scale factor. In the same way, conductor's width and spacing increase implies decrease in the inductance and DC resistance. The main drawback of this solution is noticeable space consumption.

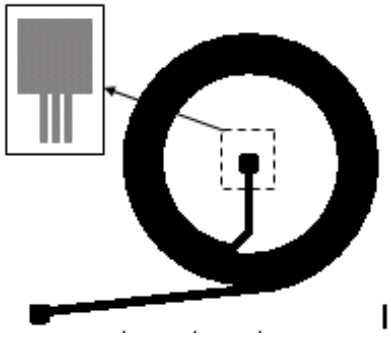


Figure 5: Interleaved conductors topology.

To obtain a DC resistance decrease with a quasi-conservation of the inductance, we propose to connect several inductors in parallel, as shown in Fig. 5. Afterwards, this structure will be named interleaved conductors.

3.2 Evaluation of equivalent resistance and inductance values

Fig. 6 presents the electrical model of two parallel-connected conductors, where L_1, R_1, L_2, and R_2 are respectively the self-inductances and DC resistances of lines 1 and 2. The equivalent resistance R_{equ} of the two lines is given by:

$$R = \frac{R_1 . R_2}{R_1 + R_2}. \tag{9}$$

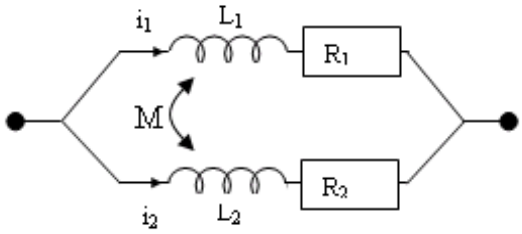


Figure 6: Electrical model of two parallel-connected conductors.

In the case of two parallel-connected conductors, assimilated to two closed lines, the inductances L_{equ1} and L_{equ2} of lines 1 and 2 are given by [18]:

$$L_{equi1} = L_1 + M \text{ and } L_{equi2} = L_2 + M \tag{10}$$

where L_1 and L_2 are the self-inductance of each inductor and M the mutual inductance defined by:

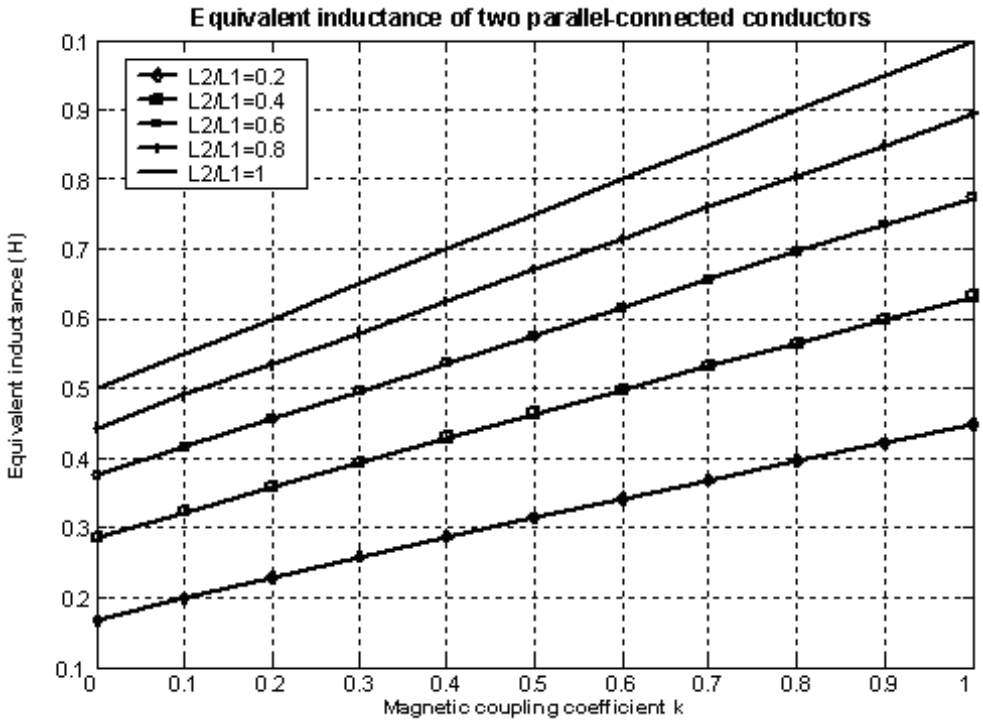
$$M = \pm k\sqrt{L_1 . L_2} \tag{11}$$

where k is the coupling coefficient which characterizes the quality of the magnetic coupling between two parallel conductors. M is positive when currents of the coupled conductors flow in the same direction. M is negative when the same currents flow in opposite directions [18]. In our case, as the two conductors are connected in parallel, M is always positive. Therefore, the equivalent inductance value L_{equ} can be expressed by:

$$L_{equi} = \frac{(L_1 + M) . (L_2 + M)}{L_1 + L_2 + M} \tag{12}$$

$$L_{equi} = \frac{L_1 . L_2 + k . (L_1 . L_2) . \sqrt{L_1 . L_2} + k^2 . L_1 . L_2}{L_1 + L_2 + 2k . \sqrt{L_1 . L_2}}. \tag{13}$$

Graphic 6 presents the results of parametric simulation of the inductance value with various coupling coefficient k and L_2/L_1 ratio. It can be easily seen that the highest equivalent inductance of two parallel connected conductors can be achieved if the magnetic coupling coefficient k and/or L_2/L_1 ratio is close the unity. This can be obtained by realizing two inductors as near as possible with similar cross sections and numbers of turns.

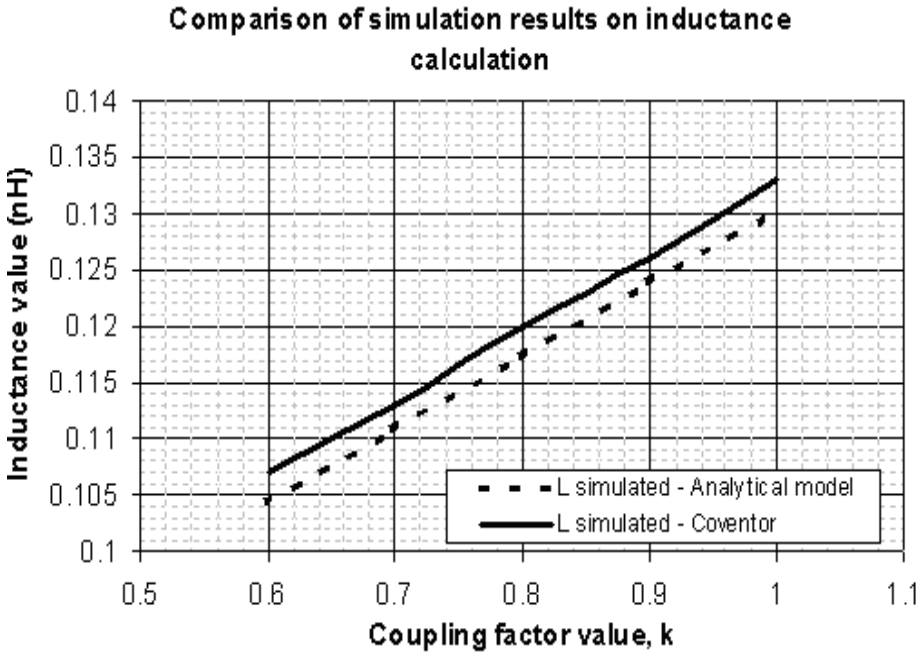


Graphic 6. Equivalent inductance of two parallel conductors.

3.3 Comparison with a single conductor inductor

Actually, different shapes of inductor, such as square, octagonal, and circular one, have been realized. Previous works have demonstrated that the circular one is the more efficient shape, as it allows, for example a better quality factor Q or more elevated working frequencies [3, 13, 17]. Therefore, several simulations have been conducted using Coventorware FEM simulation toolbox, in order to evaluate the inductance and resistance value of 1 to 5 interleaved inductors.

Our first work has consisted in validating the FEM model. For that, we have compared the inductance value L as a function of the coupling factor k obtained with the FEM model and the analytical one. Graphic 7 shows a good agreement between the analytical and numerical models.

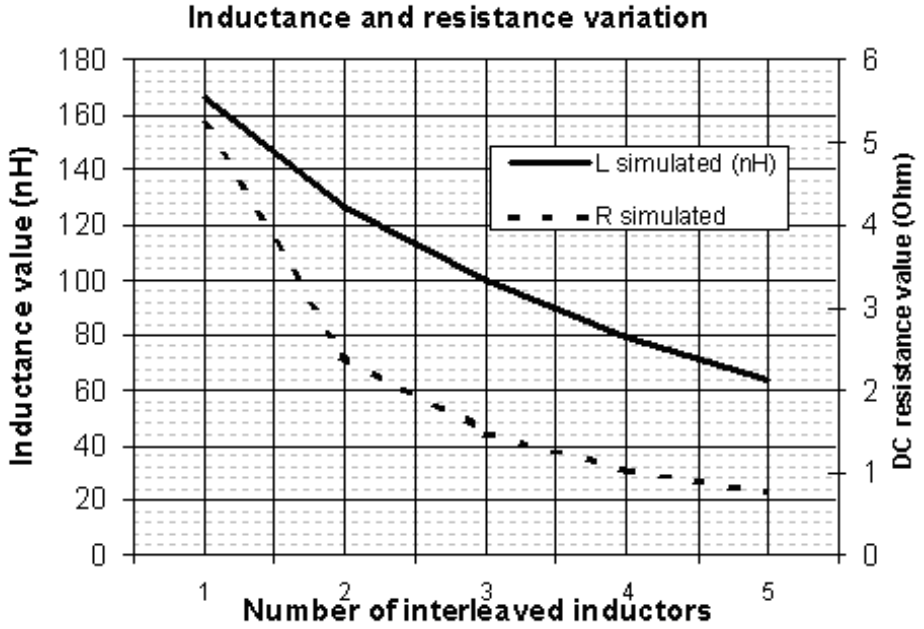


Graphic 7. Comparison of simulation results on inductance calculation.

Therefore, we have conducted simulations to evaluate the inductance and resistance behaviour as a function of the number of interleaved conductors connected in parallel. Conductors' width and spacing, as well as the external diameter, are constant for all simulations. We can observe in Graphic 8 that the use of 5 parallel connected inductors imply a 85% decrease of the resistance value. At the same time, the equivalent inductance is 61.3% lower than the one of a single inductor.

Number of conductors in parallel	Inductance (nH)	Resistance of classical inductance (Ohm)	Resistance of interleaved inductance (Ohm)
1	166	5.2	5.2
2	126.4	4.1	2.4
3	99.8	3.7	1.5
4	79.8	3.2	1.0
5	64.3	2.96	0.7

Table 1: Resistance at different number of interleaved conductors for a constant inductance value.



Graphic 8. The simulation results for inductance and resistance for n parallel-connected inductors.

Therefore, we made new simulations with Coventor to obtain a comparison of the resistance value for a constant inductance, on a same surface, using identical wire dimensions but by modifying the inductor's number of turns. Table 1 presents a comparison of the results. We can notice that, for a constant inductance value, the choice of an interleaved topology allows a significant reduction of the resistance value. As a result, interleaving conductors present a valuable solution for resistance reduction.

4 Fabrication process

Different shapes of planar inductors can be realized on a silicon wafer to validate our work. Though the square shape is the easiest in realization, we chose the circular inductor as it allows higher operation frequency than the others. For that, classical micromachining techniques have been used. Table 2 presents the geometrical parameters used in our process.

	Value (μm)
Conductors width	15
Conductors spacing	15
Conductors thickness	15
Coil's external diameter	3000
Coil's turn number	5

Table 2: Inductor' s geometrical parameters.

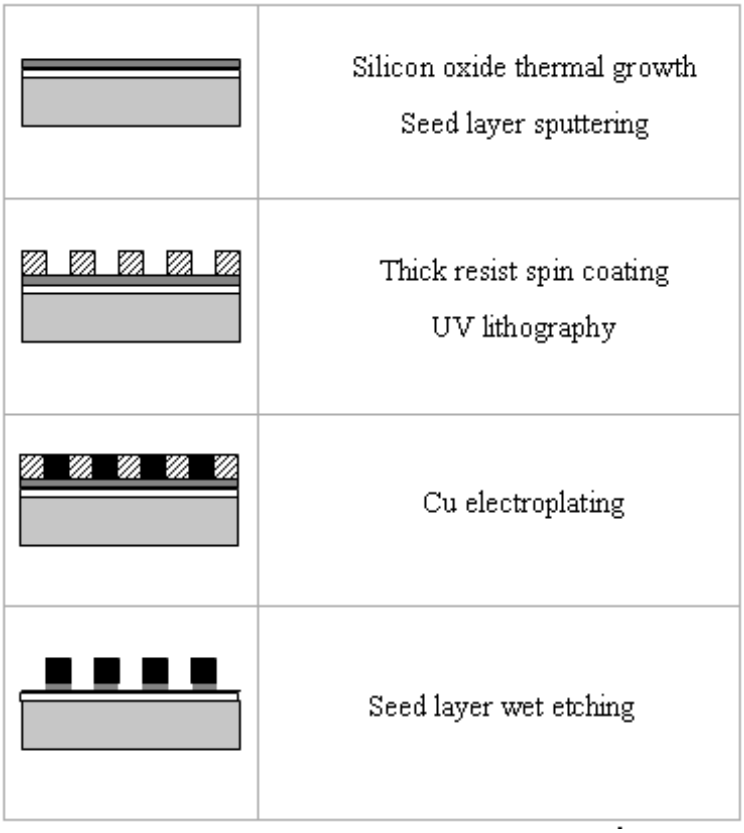
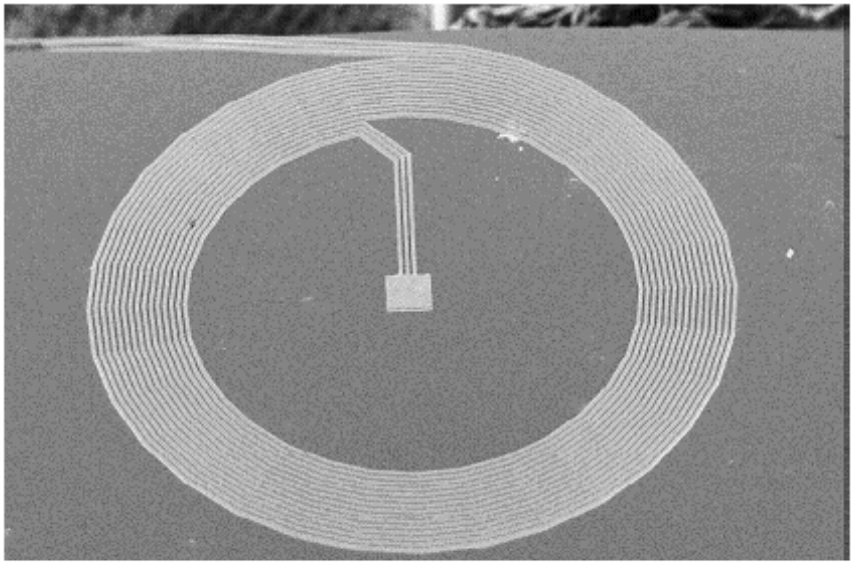
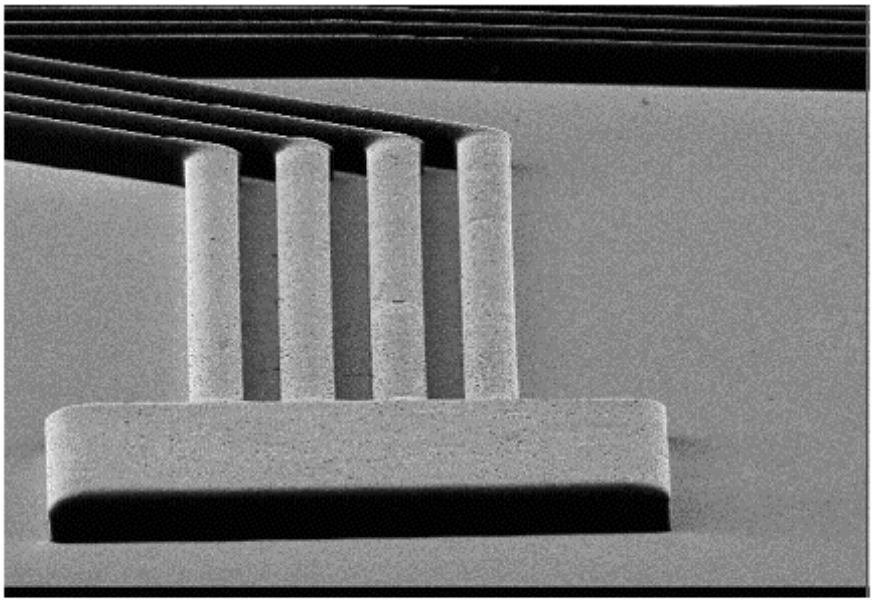


Figure 7: Technological process flow.



(a)



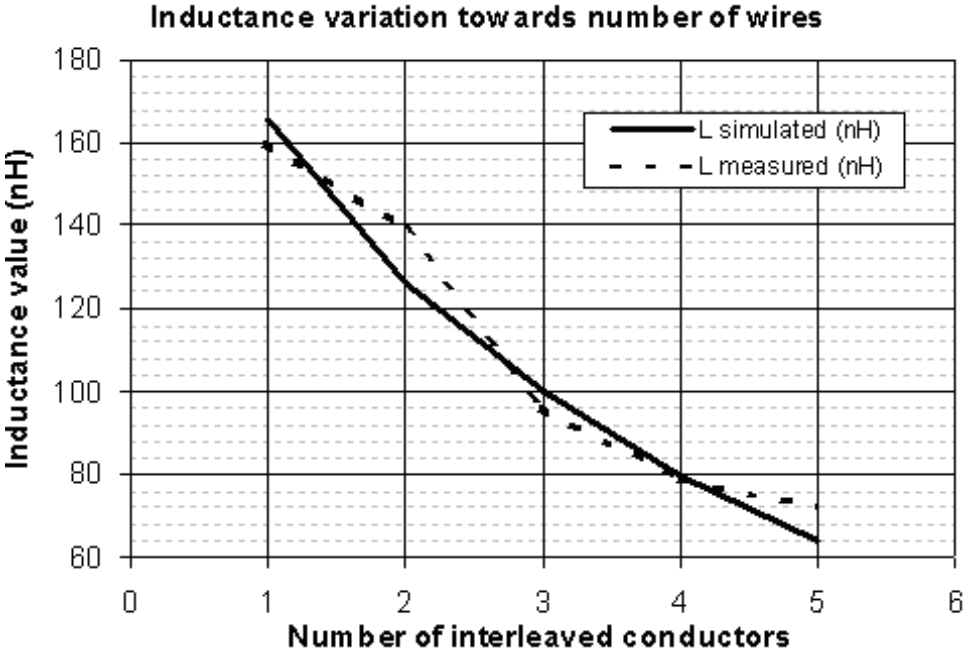
(b)

Figure 8: Examples of realization: a) global view of a circular inductor; b) details of connection with 4 interleaved inductors.

The technological process starts with a thermal growth of a silicon oxide layer to ensure a good insulation. Then, an UV lithography step is conducted using a spin coating deposition of resist. The process is optimized for thick resist deposition, around 20μm. After insulation, conductors are grown up by copper electroplating. Finally, the seed layer is removed by wet etching. Fig. 7 summarizes the technological process flow, Fig. 8 shows several pictures of the realized inductances. Fig. 8a presents the global 3 parallel-connected inductors and Fig. 8b shows details of the parallel connection realized between four interleaved inductors.

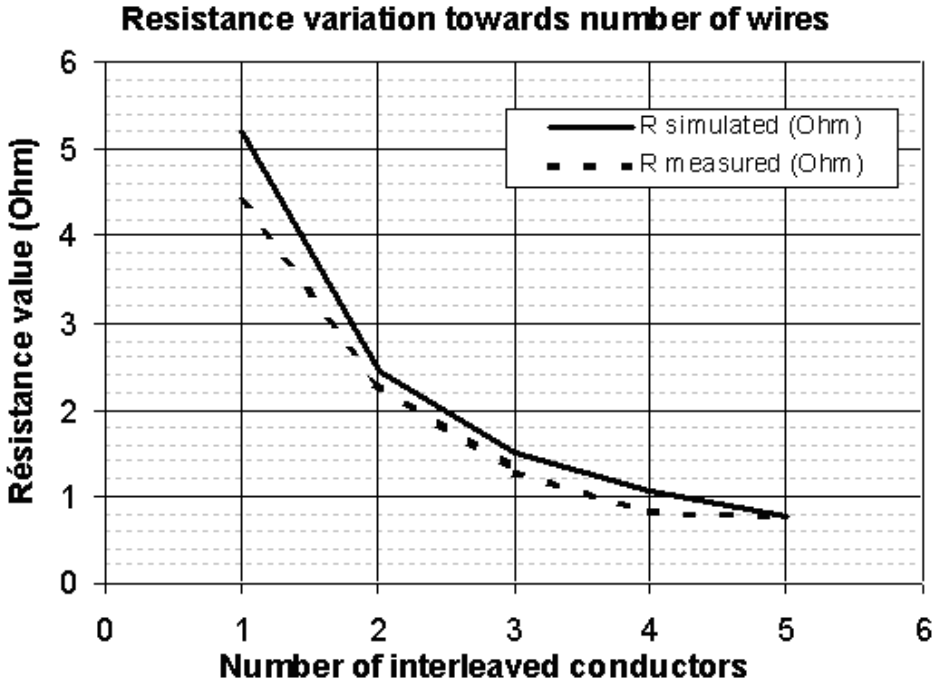
5 Characterization results

Electrical measurements were made at 1MHz to determine the inductance and resistance values. For that, the impedance analyzer HP4284A was connected to a PC via a GPIB bus. A special interface has been created using Labview software.



Graphic 9. Inductance versus the number of interleaved inductors.

Graphic 9 presents the inductance variation versus the number of interleaved inductors. A good agreement exists between the simulation results and the experimental data. However, the use of interleaved inductors implies a decrease of the inductance.



Graphic 10. Resistance versus the number of interleaved inductors.

Graphic 10 presents the resistance variation versus the number of interleaved inductors. A good agreement between theoretical and experimental results can be observed as well. Differences can be explained by the electrical conductivity of electroplated copper, different from the bulk value ($1.75e10^{-8}$Ohm.m) and variations of the width and thickness of the conductors. The decrease of the inductor resistance value by the use of interleaved conductor is then demonstrated.

6 Conclusion

We have presented a new planar inductive component topology meant for decrease of the DC resistance. The interest of interleaved conductors has justified by a DC resistance decreasing. At the same time, due to the important effect of magnetic coupling, the inductance value decrease is slowed down. This last phenomenon is demonstrated by simulating DC resistance for various inductors topologies, considering constant inductance value. Comparison of simulation results obtained with FEM toolbox Coventorware and results obtained with the analytical model, has validated the simulation tool feasibility for parallel-connected inductors inductance computation. We have seen that the same inductance can be obtained with much lower resistance value in the case of interleaved topology. Numerous inductors, connected in parallel, increase the equivalent section of conductors, allowing higher current density with the same inductance value. Then, a technological process including classical UV lithography, has been developed. Fabricated components have been characterised with an automatic test-bench. The results show a very good agreement and validate all the developed theory showing the effectiveness of interleaved topology for reduction of the inductors DC resistance.

Further improvements are in progress. On the one hand, the global structure must be improved to reach the highest possible coupling factor. On the other hand, several technological parameters are under measurement to be reintroduced in simulations.

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