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Electronic circuit simulation with ideal switches

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Abstract

A recent model of an internally or externally controlled ideal switch is described. General nonperiodical switching is considered. No limitations regarding the circuit structure and complexity are imposed. Application to variety of electronic circuits is demonstrated. Special attention is paid to electronic power circuits such as switched power supplies and converters.

Keywords: Electronics, power circuits, communication circuits, simulation, switches.

1 Introduction

Power electronic components (transistors, thyristors, and diodes) for convenience are often modeled as switches. Instances of such models may be found in switched capacitor or switched-current networks, switched power supplies, mixed signal circuits such as A/D converters [1], etc. The advantage of using ideal switches in circuit simulation is explained in [2]. To simplify, if nonideal models are used in a SPICE-like simulation, simulation of the resulting stiff system demands long simulation times. When switches are modeled as ideal, simulation for the switch transition is performed in one time instant, rather then as a step transition of voltages and currents. It

saves simulation time without significant error in the simulation results. It is our experience that in circuits where switches are predominant elements, time overheads are reduced by an order of magnitude.

Several approaches have been used for analysis of switched networks. Externally controlled switches and a restricted set of circuit elements are used in switched-capacitor (SC) networks [3, 4]. SC networks are a subset of periodically switched linear networks. Techniques to analyze such problems are described in [5] and [6]. The method described in [6] deals also with a restricted set of nonlinear networks, but such methods cannot be used for the circuits with internally controlled switches, as they appear in switched power supplies and converters [7].

One group of methods used for the time-domain simulation of internally controlled switched networks is based on the state variable formulation [8-10] and [11]. These are, however, difficult to implement in a general-purpose electronic simulation program. A summary of this class of methods can be found in [12]. Recently reported additional results [13] suffer, however, the same deficiencies related to both possibility of implementation in general purpose simulation program, and restriction to the set of circuit elements.

Algorithms of analysis of linear networks with internally controlled switches are described in [12] and [14]. The method in [14] enables simulation of linear systems where inconsistent initial conditions occur after switching. In networks with internally controlled switches, the Dirac impulses of voltage or current can cause changes of state of other switches in network. Algorithms that take this into consideration are described in [12] and [15]. It is shown that nonlinear storage elements (capacitors and inductors) must be represented by charges and fluxes.

We started our research in this field by recognizing the fact that *circuits with ideal switches*, no matter how many of them are present in the circuit, and no matter what is the structure of the circuit and the nature of the rest of the elements, *are nonlinear per se*. Or, in other words: there are no linear circuits if ideal switches are present. Nonlinear circuits are, in general, described by nonlinear equations that are unavoidably solved by iterative procedures. The switch is nonlinear as it can be, so that, the ideal switch model proposed recently [16, 17] is suitable for the time-domain simulation of networks containing externally and internally controlled switches. Our switch model is intended for use with a standard SPICE-like simulator. Namely, the switch is considered as a circuit element and managed either during circuit description, or simulator's code writing, as any other element (resistor, diode, etc.). The main motivation for this research was the fact that the current versions of the switch model implemented in SPICE are

nonideal, with low R_{on} resistance and high R_{off} resistance [18]. When finite values of switched resistance are used, however, the eigenvalues in the system are extreme, and the simulation demands very long CPU times. Switch models with energy storage elements [19] can prevent such extreme eigenvalues and the simulation becomes somewhat faster.

The structure of the paper is as follows. Our nonlinear switch model is presented in Section 2. Section 3 handles inconsistent initial conditions and Dirac impulses, and suitability of the model for simulation of nonlinear networks. In Section 4, a switch model with continuous transition of resistance between zero and infinite values is presented. The paper is concluded with a review of simulation examples demonstrating the versatility and effectiveness of the model described.

2 Nonlinear ideal switch model

2.1 Limitations of the usual ideal switch model

A closed switch connecting nodes j and k is modeled as a zero-valued voltage source

$$v_j - v_k = 0. \tag{1}$$

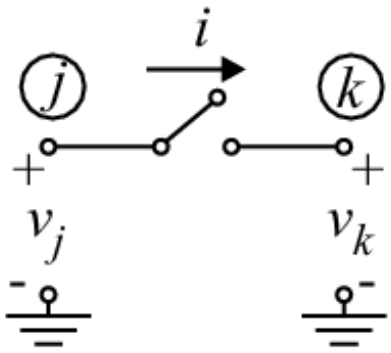
If the switch is open, the model is equivalent to a zero-valued current source:

$$i = 0 \tag{2}$$

where i is the current through the switch flowing from the node j to the node k, as depicted in Fig. 1a. Having in mind the graphical representation of (1) and (2) one readily concludes that the ideal switch is a nonlinear circuit element as it can be. Accordingly, independent of the algorithm applied for solution of the network equations related to circuits containing ideal switches, the response evaluation is performed iteratively. We here adopt the Newthon/Raphson procedure that is applied in most circuit analysis programs, and our model is expressed in such a way to be easily applicable in this kind of programs. The rest of the discussion is related to equation formulation.

Modified nodal analysis (MNA), described in [20-22], is well suited for automated formulation of the system of equations. For each component, a model stamp is developed. Since (1) is a voltage equation, and (2) is a current equation, two different stamps should be defined for the switch [21, 23]. Fig. 1b depicts the stamp for closed switch, corresponding to (1), where z is the system matrix index of the variable i. When the switch is

open, it is simply omitted from the system of equations. However, if we want to introduce the current i as a variable, to have the same set of variables as in the case of closed switch, than the stamp given in Fig. 1c may be used. When implemented, this stamp may be simplified by omitting the contributions to rows j and k since the current leaving these nodes is zero.



(a)

	v_j	v_k	i	rhs
j			1	
k			-1	
z	1	-1		

(b)

	v_j	v_k	i	rhs
j			1	
k			-1	
z			1	

(c)

Figure 1: Ideal switch (a) and stamps representing the model of (b) closed and (c) open ideal switch. The right hand side vector of the system of equations is denoted as rhs.

It would seem that one could replace one stamp by another when the switch transition occurs. Unfortunately, this leads to numerical problems in a SPICE-type program, since the switch transition changes the network topology, and this is reflected in the change of the structure of the nonzero

entries in the system matrix. If such models were implemented, a new reordering and pivoting in the matrix would be necessary after every switch transition.

2.2 Nonlinear model of a closed switch

Our first concern is to define the switch model that would have the same structure of nonzero entries for both states [16, 17]. Let us first consider a closed switch. The problem here is that the zero entry appears on the main diagonal of the matrix. However, for circuit simulation (1) can be replaced by

$$(v_j - v_k) - ri = -ri^m \tag{3}$$

where r is a new model parameter with dimension of resistance. Superscript m denotes the iteration number, and i^m denotes the value of the current obtained in the previous iteration. When convergence is reached, the current in $(m+1)$th iteration equals that from mth iteration:

$$i = i^m \tag{4}$$

and one obtains the equation for the closed switch (1). We will use the simple circuit of Fig. 2a to illustrate this procedure. The iterative process of switch closing is depicted in Fig. 2b in $i - v$ coordinate system. At the beginning the switch is open - that is at the point B in Fig. 2b. When convergence is reached, the switch should be closed (point A). If the model given by (3) is used, transition from B to A is defined by iterative procedure through the intermediate solutions B', B'', B'''. These points are determined by the line $A - B$ and another line, representing the switch model equation. Convergence is faster when lower values or r are used. Nevertheless, too low value of parameter r could lead to numerical problems. We have found that the value of $10^{-5}\Omega$ enables fast convergence and is high enough to avoid numerical problems.

The stamp describing the model is given in Fig. 3a and contains no zero on the main diagonal.

To visualize the model, we can compare the convergence process with the time-domain simulation of a linear inductor. If m denotes time instant, parameter r can be replaced with L/h, where L is "inductance" and h is "time step". From (3), one would obtain the equation

$$v_j - v_k - \frac{L}{h}i = -\frac{L}{h}i^m. \tag{5}$$

This is the linear inductor's companion model, $v_{jk} = L(di/dt)$, where discretization is performed by the use of backward Euler formula. When steady-state is reached, the inductor turns out to be a short circuit. We have transferred this property into the iterative domain, i.e. reaching the convergence. In other words, closing the switch is modelled by replacing the switch by a quasi-inductor. The whole transition of the switch is performed as an iterative process in one time instant.

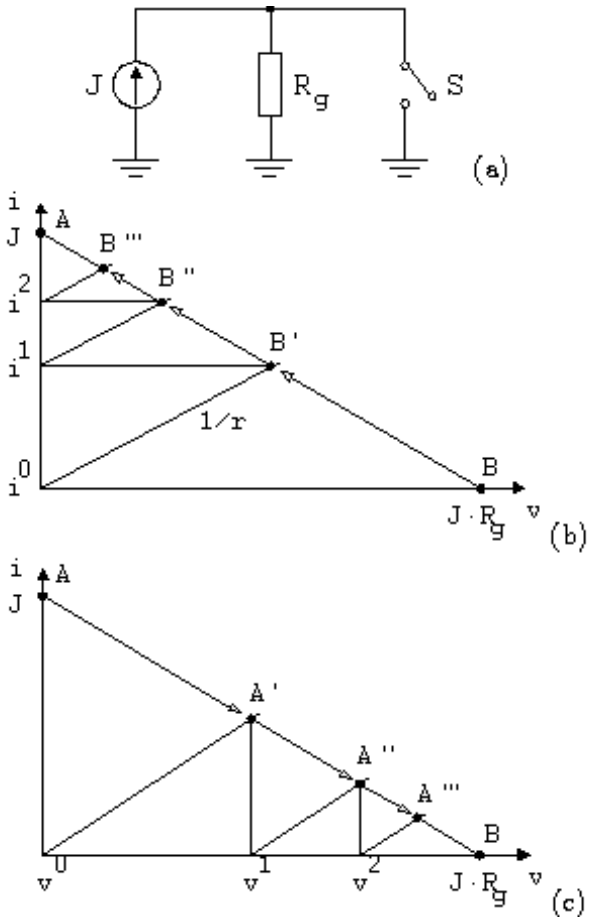


Figure 2: a) Simple circuit with a switch and b) iterative procedure of switch closing. The switch current in the mth iteration is i^m and $1/r$ is the slope of the line representing the switch model. c) Iterative procedure of switch opening. The switch voltage in the mth iteration is v^m. $1/R$ is the slope for the open switch.

	v_j	v_k	i	rhs
j			1	
k			-1	
z	1	-1	$-r$	$-ri^m$

(a)

	v_j	v_k	i	rhs
j			1	
k			-1	
z	1	-1	$-R$	$v_j^m - v_k^m$

(b)

Figure 3: Stamps implementing the nonlinear model of (a) closed switch and (b) open switch. The structure of nonzero entries is the same in both cases, and no zero entries are generated on the main diagonal.

2.3 Nonlinear model of an open switch

For the open switch we introduce a new model

$$v_j - v_k - R \cdot i = v_j^m - v_k^m \tag{6}$$

where R is a model parameter with the dimension of resistance. When the convergence is reached, the voltages from $(m+1)$th and mth iteration are equal

$$v_j = v_j^m \quad , \quad v_k = v_k^m \tag{7}$$

and from (6) one obtains (2) which models the open switch.

The iterative procedure of switch opening is again illustrated using the circuit in Fig. 2a. At the beginning the switch is closed, and the circuit solution is in position A. The transition from A to B goes trough the points A', A'', A''' in Fig. 2c. The convergence will be reached in smaller number of iterations if R is higher but too high value could lead to numerical problems. We found the value of $10^9\Omega$ convenient.

With our choice of r and R, the number of iterations necessary for convergence of nonlinear switched networks is not affected by our switch model being determined by other nonlinear devices in the network.

The stamp that corresponds to the model (6) is given in Fig. 3b. The structure of the nonzero entries in the stamp is the same for both switch states.

We can use the same analogy to visualize our model. In the time-domain, the corresponding equation is a linear capacitor model. When the convergence is reached, the current through the quasi-capacitor is zero.

With the model given in Fig. 3 we have obtained switch transitions that change the network topology but not the structure of nonzero entries in the sparse matrix. Reordering of the matrix after switch transition is not necessary. The use of nonlinear switch model requires iteration even if the rest of the network is linear but the convergence is reached quickly and while the algorithms for iterative solutions of nonlinear networks are built into any SPICE type program. When analyzing nonlinear networks, our nonlinear switch model does not noticeably increase the number of iterations.

3 Inconsistent initial conditions

Inconsistent initial conditions can occur in networks with ideal switches. An example is given in Fig. 4. If the switch is in position 1, capacitor C_1 is charged to the voltage E, and C_2 has zero voltage. When switch transition occurs from 1 to 2, a Dirac impulse of current appears, and instantaneously equalizes the voltages.

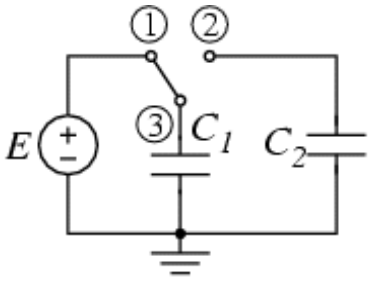


Figure 4: Circuit with inconsistent initial conditions.

In [12, 14] and [15], the problem of inconsistent initial conditions is resolved by a special integration procedure. When our switch model is used, consistent network state after switch transition can be found as well. Fig. 5 shows the simulation results for the circuit in Fig. 4. The switching period is 4ms and the capacitor values are $C_1 = C_2 = 100$nF. After the switch

transition from 1 to 2 ($t = 2$ms), some charge is instantaneously transferred through the switch, and the total amount of charge in the circuit is conserved. No special techniques are necessary for finding consistent initial conditions after the switching.

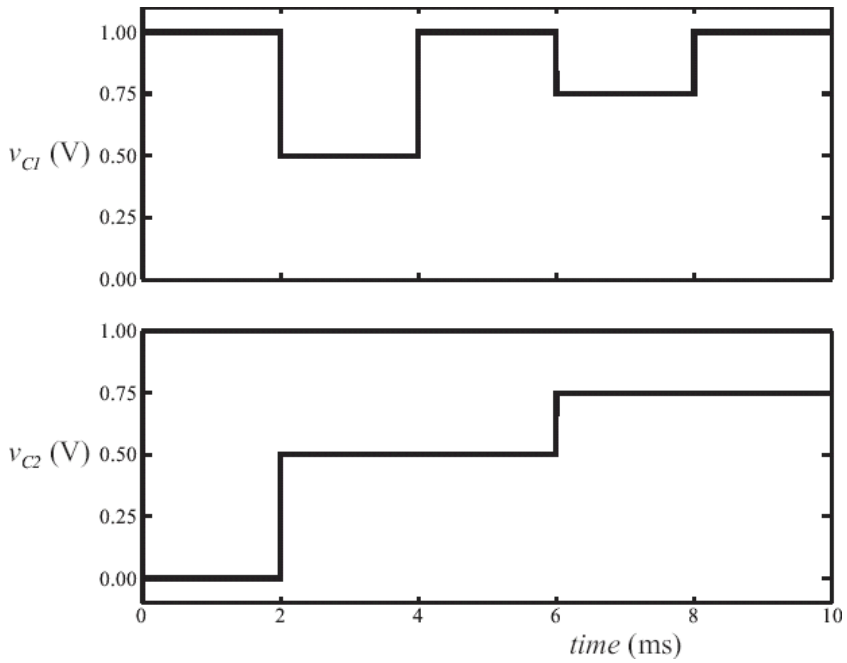


Figure 5: Circuit with inconsistent initial conditions.

With our model, the switching is not represented just as a replacement of one network topology by another. The switch transition is modelled through a number of iterations, where in every iteration both Kirchhoff laws are satisfied. The values of voltage and current in the previous and new iteration are always connected by quasi-capacitor or quasi-inductor model. For that reason, a finite amount of charge is transferred from C_1 to C_2 in every iteration and charge conservation is maintained. In the dual problem, current through the inductor would be instantaneously changed, and our nonlinear ideal switch model conserves the flux in the network.

As discussed in [12] and [15], the problem of inconsistent initial conditions is not only to conserve the charge and the flux. It is important to take into account Dirac impulses that can occur at the instant of switching. The problem will be explained for the ideal buck-boost switching converter

[19, 24] given in Fig. 6a. The switch S represents the transistor that is externally controlled. The diode is represented as an ideal internally controlled switch. One can model this diode using a control variable p:

$$D : \begin{cases} \text{closed}, & \text{if } p > 0 \\ \text{open}, & \text{if } p < 0 \end{cases}$$
$$p = \begin{cases} i, & \text{if } D \text{ is closed} \\ v_j - v_k, & \text{if } D \text{ is open.} \end{cases} \tag{8}$$

Therefore, p is an internal circuit variable and its value is determined in every iteration.

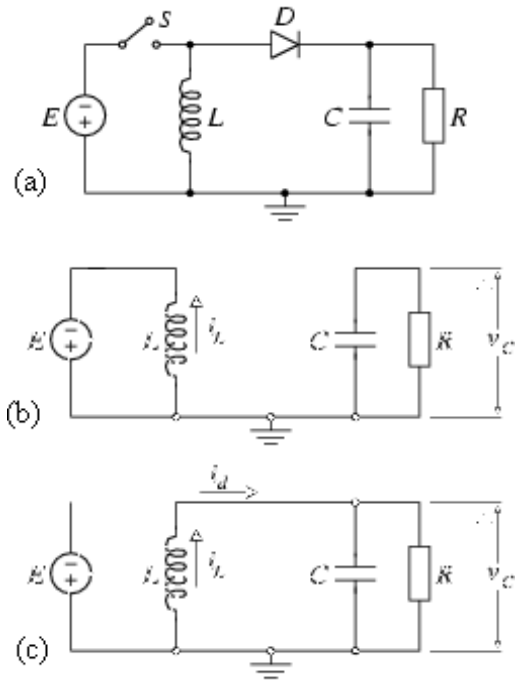


Figure 6: a) Ideal buck-boost switching converter. b) Equivalent circuit for S closed and D open. c) Equivalent circuit for S open and D closed.

When switch S is closed and switch D open, the circuit is shown in Fig. 6b and inductor current i_L is linearly increasing. When S is externally opened, i_L has no closed loop and drops instantaneously to zero, and a Dirac impulse voltage appears on the inductor. It changes the switch control

variable p to a positive value, and D closes. When this happens, the inductor current has a closed loop, Fig. 6c, and there is no discontinuity in its value. There is no impulse of the inductor voltage but the Dirac impulse is needed to switch the diode D, i.e., to change the value of the control variable p.

A similar condition occurs when S is closed again. If i_L has not decayed to zero, D is still closed and the capacitor is connected to the voltage source through S and D. A Dirac impulse of current flows through the capacitor, the switches S and D, and the voltage source. This current impulse flows in opposite direction through D, and changes the control variable p to a negative value. This opens diode D at the same time instant as S is closed, and, as a consequence, the capacitor is not directly connected to the voltage supply in any time instant.

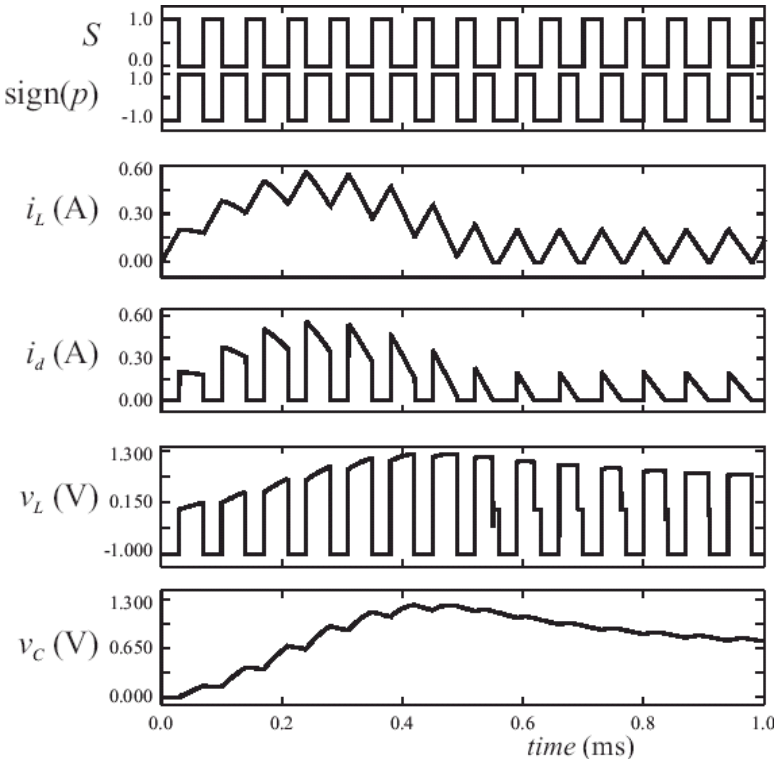


Figure 7: Simulation results for the buck-boost converter.

Simulation results for the buck-boost converter with our switch model are presented in Fig. 7. The element values are $E = 1\text{V}$, $L = 150\mu\text{H}$,

$C = 50\mu$F, and $R = 10\Omega$. The switching period for S is 70μs, and the duty cycle was 3/7.

To conclude this consideration, one may say that our model takes into account the Dirac impulse, although no explicit methods are used for that. With our model, one obtains Dirac impulse with very high number (amplitude) after the first iteration. Since the solution from one iteration is used to determine the conditions for the next iteration, this Dirac impulse can change the states of the internally controlled switches in the circuit.

4 Model of the switch with two thresholds

The switch modelled by stamps in Fig. 3 can be externally or internally controlled. For the internally controlled switch, a control variable (voltage or current) is needed. In all examples until now, we have assumed that the control voltage has one threshold value. The switch, however, may be implemented with two thresholds, V_{on} for closing switch, and V_{off} for opening. Such control is presented in [18], where switch is implemented with finite resistance, R_{on} for closed switch ($V_c > V_{on}$) and R_{off} for the open ($V_c > V_{off}$). When the control voltage is between the thresholds, the switch resistance R has continuous transition between R_{off} and R_{on}.

In our model, the switch is ideal. The stamp for the closed switch behaves as $R_s = 0$ and for the open switch as $R_s = \infty$. Nevertheless, continuous transition of the switch resistance between zero and infinite values can be also modelled. If V_c is between V_{on} and V_{off}, the following switch model is used

$$v_j - v_k - [R \cdot x - (1 - x)] \cdot i = (v_j^m - v_k^m) \cdot x - r \cdot i^m (1 - x). \tag{9}$$

The parameter x is a function of the control voltage. We have implemented x as

$$x = 0.5 + 2 \cdot \left(\frac{V_c - V_a}{V_d} \right)^3 - 1.5 \cdot \frac{V_c - V_a}{V_d} \tag{10}$$

where

$$V_a = \frac{V_{on} + V_{off}}{2} \text{ and } V_d = V_{on} - V_{off}. \tag{11}$$

Both x and $\partial x / \partial V_c$ are continuous functions of V_c. An overview of switch control functions is given in [18]. The stamp corresponding to (9) is given in Fig. 8. As can be seen, the structure of nonzero entries is the same as for the open and for the closed switch.

	v_j	v_k	i	rhs
j			1	
k			-1	
z	1	-1	$-Rx$ $-r(1-x)$	$(v_j^m - v_k^m)x-$ $ri^m(1-x)$

Figure 8: The stamp for the switch whose state is between open and closed (with finite resistance).

When $V_c \leq V_{off}$, parameter x acquires the value 1, and the stamp given in Fig. 8 reduces to the one of Fig. 3b. If $V_c > V_{off}$, the value of x becomes zero, and the stamp becomes equal to that of Fig. 3a. If V_c is between V_{off} and V_{on}, x has the value in the range (0,1). When convergence is reached, $v = v^m$ and $i = i^m$. From (6) one can obtain the switch resistance as the voltage-to-current ratio:

$$R_s = \frac{x \cdot R}{1-x}. \tag{12}$$

The stamp given in Fig. 8 can also be applied to problems other than the switch modelling. It can model extreme parameter values, while the contribution to the system matrix is neither too low nor to high.

5 Simulation examples

5.1 The hybrid Ćuk converter

We will continue our review of simulation examples by examining the recently proposed hybrid Ćuk converter with four capacitors [25]. It is an improved version of the original Ćuk converter. The circuit schematic is depicted in Fig. 9.

Simulation of this circuit was performed by the Alecsis simulator [26-28]. Simulation results are depicted in Fig. 10. Here, the responses of the load current and the load voltage to a step of input voltage are presented. The switches are externally controlled at rate of f_s = 50kHz. The simulated circuit elements are V_{in} = 12V, D = 0.75, L_{in} = 600μH, L_0 = 600μH, $C_1 = C_2 = C_3 = C_4$ = 22μF, and C_0 = 1μF. These parameters are not optimized from the point of view of circuit performance. For this simulation nominal time-step value of $t_0 = 0.01\mu$s was used.

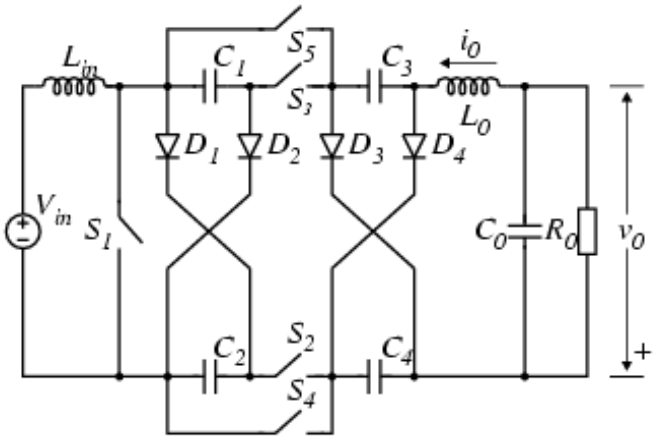


Figure 9: The new hybrid Ćuk converter with four capacitors [25].

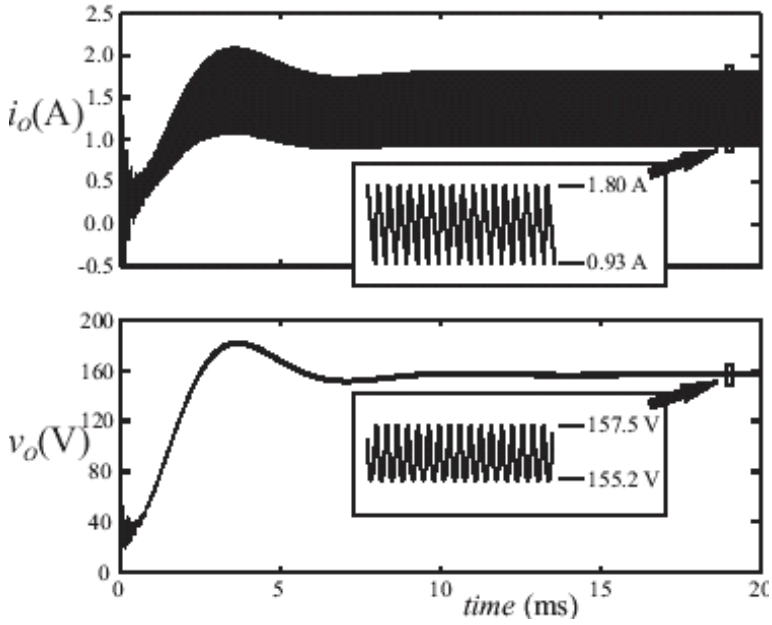


Figure 10: Simulation results (step response) for the circuit of Fig. 9. Top: load current, bottom: load voltage.

5.2 Second order sigma-delta converter

The next example is related to simulation of complex mixed-signal circuits that are nowadays frequently encountered in telecommunication and measurement setups. Namely, one is to deal with structures containing analogue circuits (described by ordinary differential equations), switches (representing elements described by Dirac impulses), digital functional elements (described by discrete equations or by tables), and in many cases, transmission lines, microelectromechanical and/or magnetic elements (that are described by partial differential equations) [29]. Here we are demonstrating the application of our switch-model to an one-bit second order sigma-delta modulator [30] as depicted in Fig. 11.

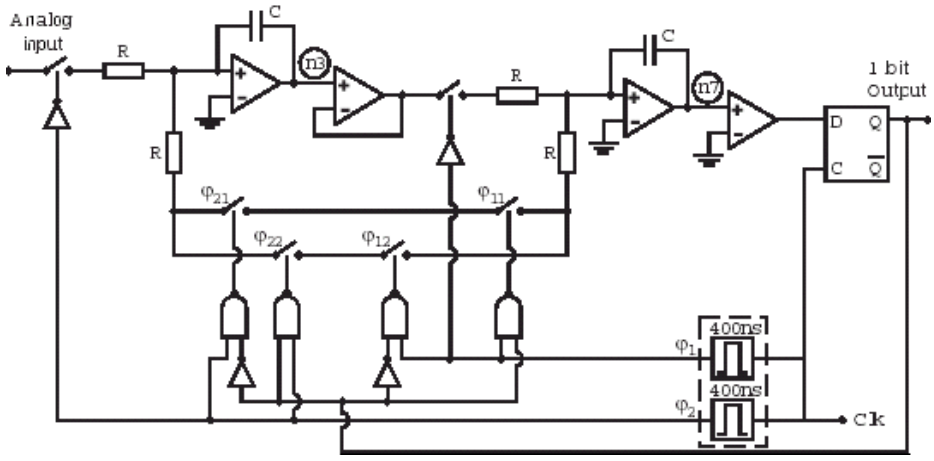


Figure 11: Second order sigma-delta A/D converter.

Simulation was again performed by Alecsis and the results are given in Fig. 12. The A/D converter is excited by a voltage ramp, the output being a pulse train digitally representing the input. The element values and the commutation scheme may be found in the original literature.

5.3 Application to testing and diagnosis

A specific application of the ideal switch is the fault modelling of electronic circuits [31]. Here the switch may be implemented to model permanent short, permanent open, stuck-at, and the most interesting intermittent faults. The procedure of fault insertion is simple. One should insert a switch

wherever one intend to create a fault. Then simulations are performed for the original circuit (the state of the switches are as if no defects are present) and for the faulty circuit (the states of the switches are changed one at a time to model the defects). If large number of defects are to be simulated in order to create fault coverage for a given test signal or in order to create a fault dictionary for diagnostic purposes, simulation time becomes crucial, especially for complex nonlinear dynamic circuits. Here, effective model of the switch is necessary.

As an example, we inserted a fault in the circuit of Fig. 11. The fault is: switch φ_{11} stuck-at-open. Instead of giving the new simulation results for the faulty circuit, we are presenting here the spectrum of the output signal obtained by Fast Fourier Transform (FFT) of the simulation results for the fault-free (Fig. 13) and the faulty (Fig. 14) circuit. Sinusoidal input signal of 10kHz was implemented. The clear discrepancy of these two spectra may be effectively used for both testing and diagnostic purposes.

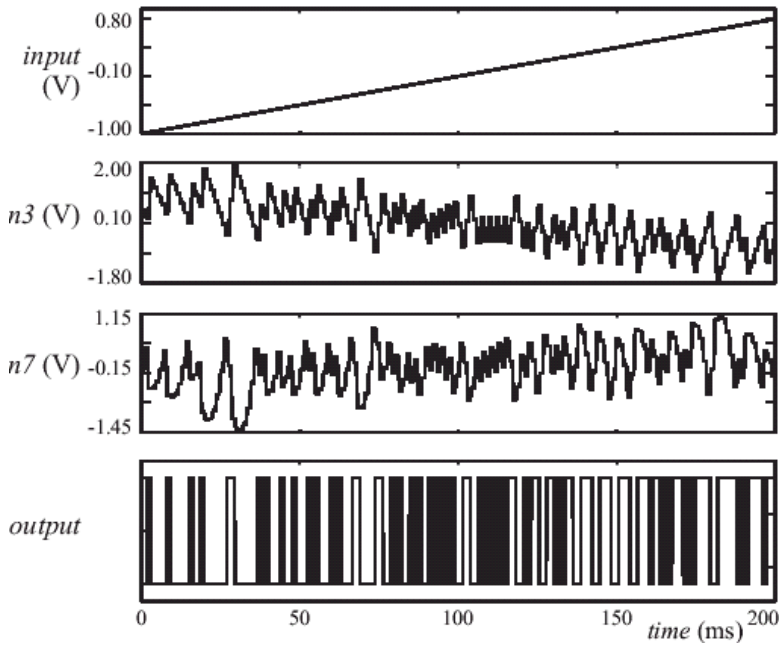


Figure 12: Simulation results for the circuit of Fig. 11.

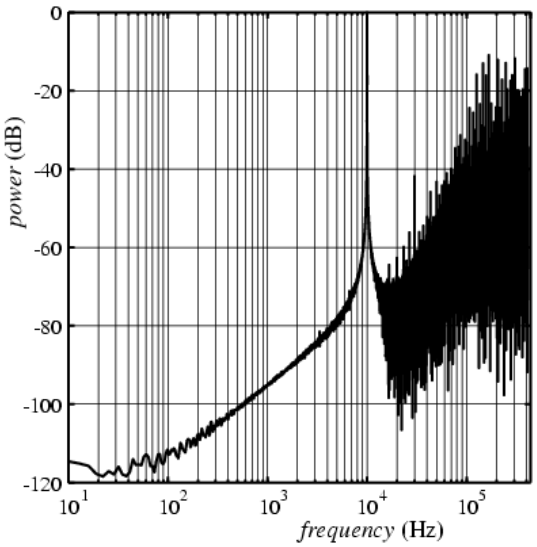


Figure 13: The response spectrum of the circuit of Fig. 11.

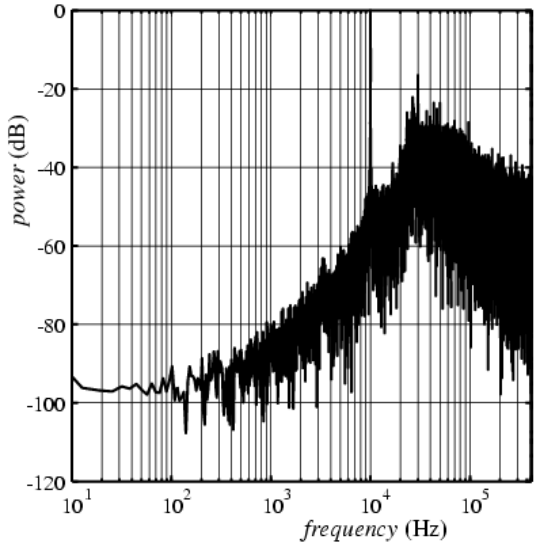


Figure 14: The response spectrum of the circuit of Fig.11 with fault inserted.

6 Conclusion

Considering the fact that any circuit containing ideal switch is nonlinear, we developed a model for the ideal switch that is applicable in a general-purpose time-domain circuit simulation program. The switch is considered as a circuit element and used by routine as simple as any other circuit element. One of the important properties of the model is that it handles real situations such as managing the Dirac pulse that is encountered when switching real circuits. Here, a set of examples is presented expressing, to our opinion, the effectiveness of the model and its versatility.

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