HAIT Journal of Science and Engineering B, Volume 2, Issues 3-4, pp. 283-304

CHAPTER 1. NEW TOPOLOGIES IN DC-DC AND AC-DC CONVERTERS

1.8-MHz, 48-V resonant VRM

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Received 1 March 2005, accepted 30 June 2005

Abstract

Recently, a new high-frequency resonant-converter technology with phase-shifted regulation has been introduced. Higher switching frequencies enable controls with higher bandwidth feedback, which in turn require less output capacitance. As a result, only surface mount ceramic capacitors can be used at the output, which are less expensive and potentially more reliable than the commonly used electrolytic and tantalum capacitors. The new technology is employed in the development of a 1.8-MHz, 48-V, 130-W (0.95-1.7 V, 100 A) resonant VRM. Fundamentals of the new technology are reviewed. Implementation details and experimental results are given.

1 Introduction

To further increase the processing speed and efficiency, future generations of microprocessor systems require lower operating voltages (below 1 V) at higher load currents (above 130 A) with high slew rates (up to 150 A/μs) [1]. High load currents with high slew rates and tighter output-voltage regulation windows require voltage regulation modules (VRMs) with fast transient responses. To achieve a fast transient response, the power conversion must be performed at higher switching frequencies (above 1 MHz). Higher switching frequencies enable controls with higher bandwidth feedback, which in turn require less output capacitance. As a result, only surface mount ceramic capacitors can be used at the output, which are less expensive and potentially more reliable than the commonly used electrolytic and tantalum capacitors. Further, at increased power levels, the 48-V distribution bus voltage is more feasible than the 12-V distribution bus voltage in order to keep the distribution losses low, especially for the high-end server and workstation applications [2]. To meet all these requirements, new high-performance VRM topologies and control technologies are needed.

Recently, a new high-frequency (HF) resonant-converter technology with phase-shifted regulation has been introduced [3, 4]. The new HF resonant technology has proven to be a cost-effective solution for VRMs for the next generation of microprocessor systems. The new HF resonant-converter technology with phase-shifted regulation is employed in the development of a 1.8-MHz, 48-V, 130-W (0.95-1.7 V, 100 A) resonant VRM.

The paper is organized as follows. In Section 2, fundamentals of the new HF resonant-converter technology are reviewed. In Section 3, implementation details of the 1.8-MHz, 48-V, 130-W resonant VRM are presented. Experimental results are provided in Section 4.

2 Fundamentals

The simplified circuit diagram of the new resonant converter with phase-shifted regulation is shown in Fig. 1. The primary-side half-bridge (HB) inverter operates in open loop with 50% duty cycle and generates a rectangular (trapezoidal) ac voltage. The secondary-side current-doubler rectifier uses synchronous rectifiers Q_1 and Q_2. Diodes D_1 and D_2 represent the body diodes of the synchronous rectifiers. For the resonant operation, an external inductor L_{ext} is added in series with the transformer primary winding, and capacitors C_1 and C_2 ($C_1 = C_2 = C$) are added in parallel to the

synchronous rectifiers.

The basic operation of the new resonant converter can be explained by using the simplified equivalent circuit shown in Fig. 2. The equivalent circuit in Fig. 2 is obtained by replacing the output-filter inductors L_{F1} and L_{F2} and output-filter capacitor C_F with current sources $I_o/2$ and voltage source V_o, respectively, and by replacing the primary-side HB inverter with a rectangular ac voltage source, and, finally, by transferring the whole primary-side circuit to the secondary side. It is assumed that synchronous rectifiers Q_1 and Q_2 are ideal, except for their output capacitances, which are included into the parallel resonant capacitances C_1 and C_2. It is also assumed that the magnetizing inductance of transformer T_1 is sufficiently large, so that it can be neglected, while the leakage inductance of the transformer is lumped with external inductance L_{ext}. The total primary-side inductance is denoted as resonant inductance L_r, as shown in Fig. 2.

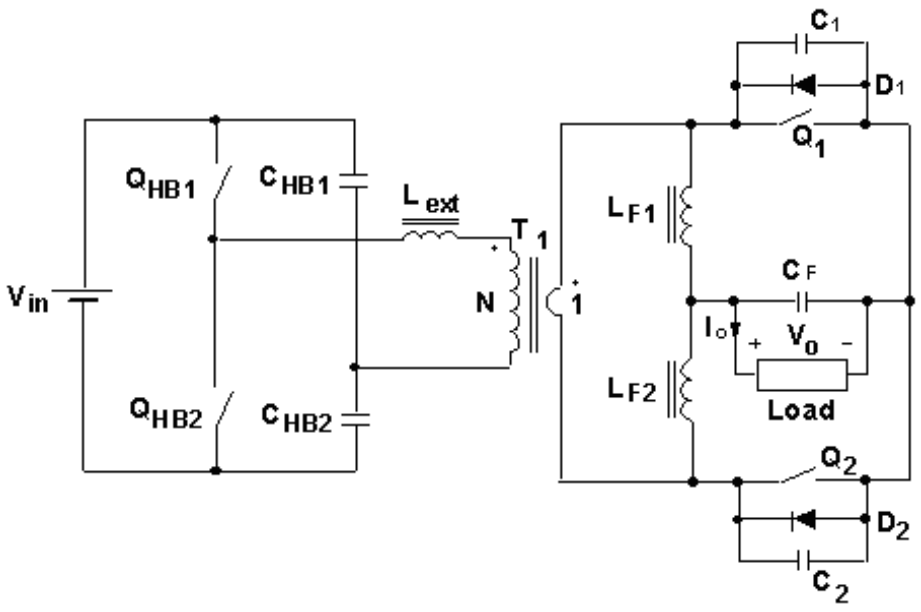


Figure 1: Simplified circuit diagram of the new resonant converter.

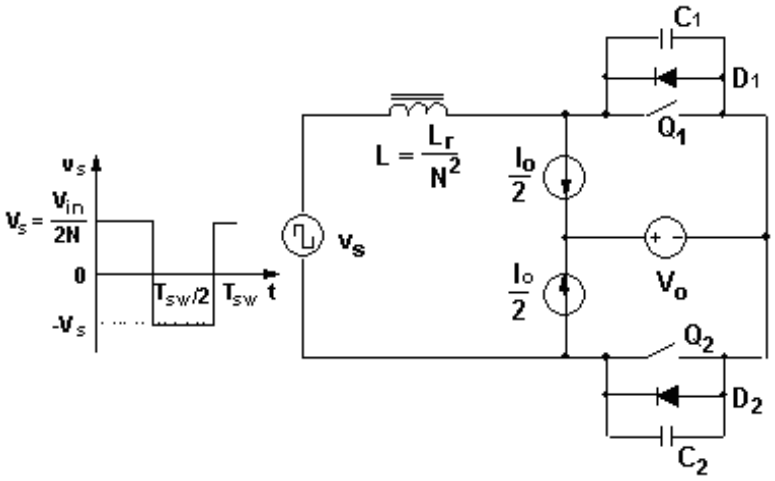
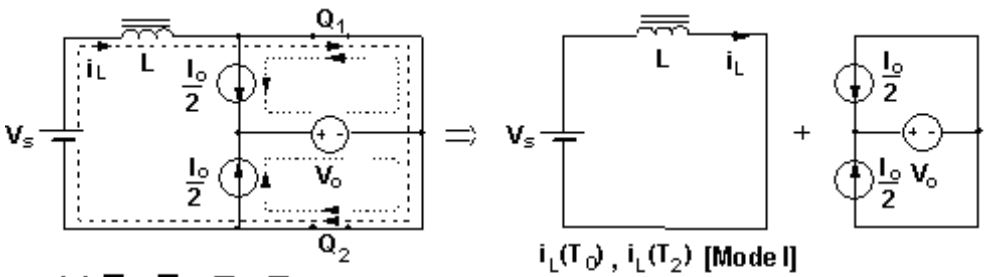


Figure 2: Simplified equivalent circuit of the new resonant converter.

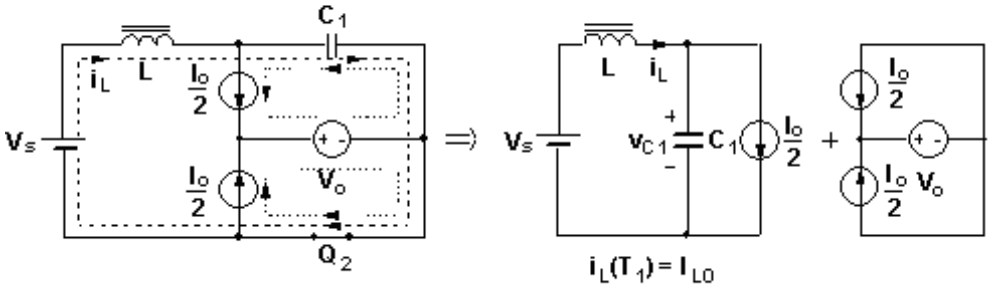
Under steady-state operation, six topological stages can be identified within a switching cycle T_{sw}, as shown in Fig. 3 [5]. These six topological stages can be arranged in two modes of operation. In the first mode of operation, the sequence of topological stages is (a)→(b)→(a)→(d)→(e)→(d), while in the second mode of operation the sequence of topological stages is (a)→(b)→(c)→(d)→(e)→(f). Key waveforms in the two modes of operation are presented in Figs. 4 and 5. In Mode I, shown in Fig. 4, the resonant voltage on capacitors C_1 and C_2 reaches zero before the ac voltage source v_s changes direction, while in Mode II, shown in Fig. 5, the resonant voltage on capacitors C_1 and C_2 reaches zero after the ac voltage source v_s changes direction. In Fig. 4, the solid-line and dotted-line waveforms of inductor current i_L and capacitor voltages v_{C1} and v_{C2} illustrate the operation at maximum load and zero load, respectively. In Fig. 5, only the waveforms at maximum load are presented. Initial values of inductor current i_L and capacitor voltages v_{C1} and v_{C2} in each topological stage are also shown in Fig. 3.

The output voltage is obtained as the average voltage across capacitor C_1 (or C_2) during a switching period T_{sw} [5],

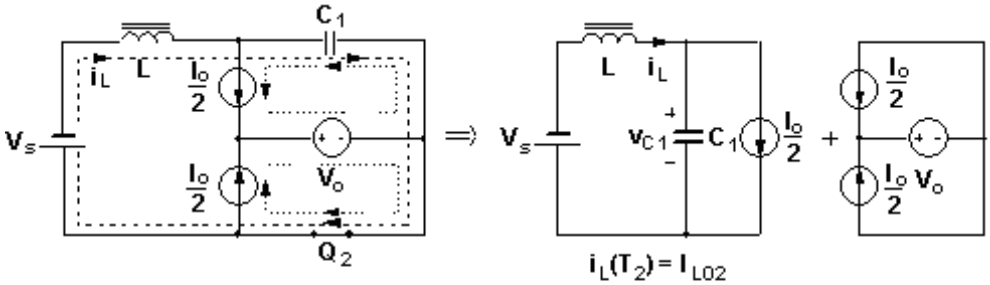
$$V_o = \frac{V_s}{\pi} \cdot \frac{T_o}{T_{sw}} \left(\frac{\pi}{2} + \operatorname{atan} \frac{V_s}{Z_c \Delta I} + \frac{Z_c \Delta I}{V_s} \right) \tag{1}$$



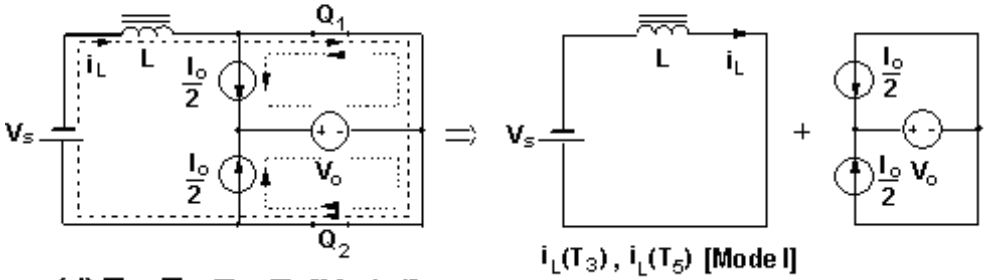
(a) $T_0 - T_1$, $T_2 - T_3$ [Mode I]



(b) $T_1 - T_2$



(c) $T_2 - T_3$ [Mode II]



(d) $T_3 - T_4$, $T_5 - T_6$ [Mode I]

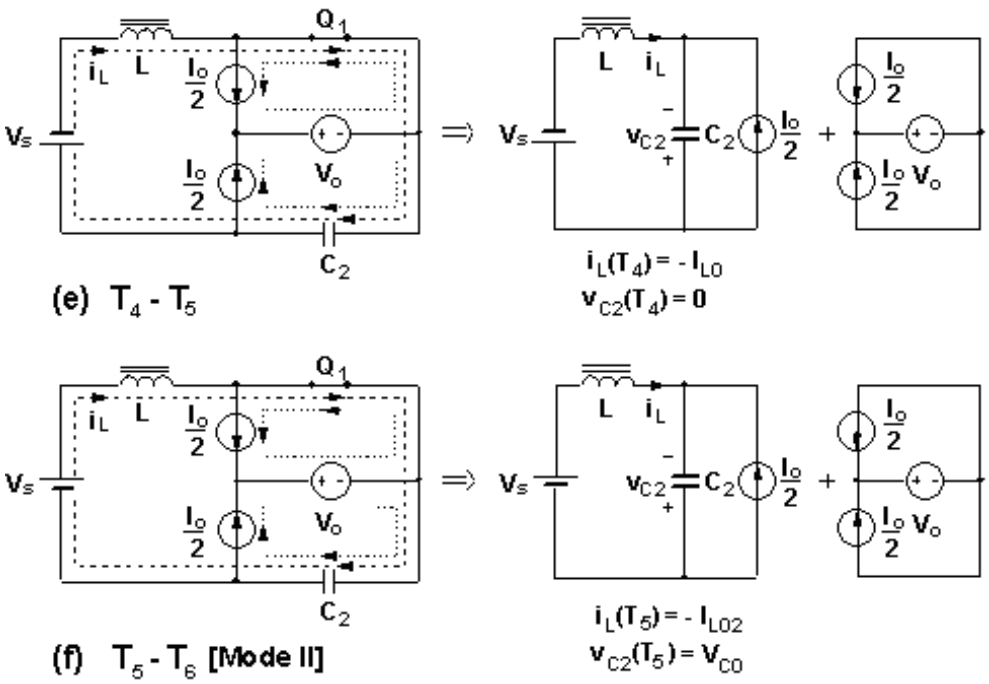


Figure 3: Topological stages.

where $T_o = 2\,\pi\,\sqrt{LC}$ is the resonant period, $Z_c = \sqrt{L/C}$ is the characteristic impedance of the series resonant circuit, and $\Delta I = I_{L0} - I_o/2$ is the ac component of the resonant inductor current i_L at the beginning of the resonant interval T_r, as shown in Fig. 4 (I_{L0} is the total inductor current at the beginning of the resonant interval T_r). It follows from (1) that the regulation of output voltage V_o versus load current, at a constant input voltage V_s, can be achieved by keeping ΔI constant. With increasing I_o, I_{L0} should also increase in order to keep ΔI constant. The output voltage regulation versus load current is illustrated in Fig. 4. The waveform of the ac component of the inductor current i_L during the resonant interval T_r is the same at I_{omax} and $I_o = 0$. Therefore, the corresponding waveforms of the resonant-capacitor voltage at I_{omax} and $I_o = 0$ are identical. Consequently, the output voltage is the same at I_{omax} and $I_o = 0$. However, the waveforms of the inductor current and capacitor voltage at I_{omax} are phase shifted compared to the corresponding waveforms at $I_o = 0$. In fact, with increasing load current the resonant interval T_r is more phase shifted with respect to the beginning of a half switching cycle.

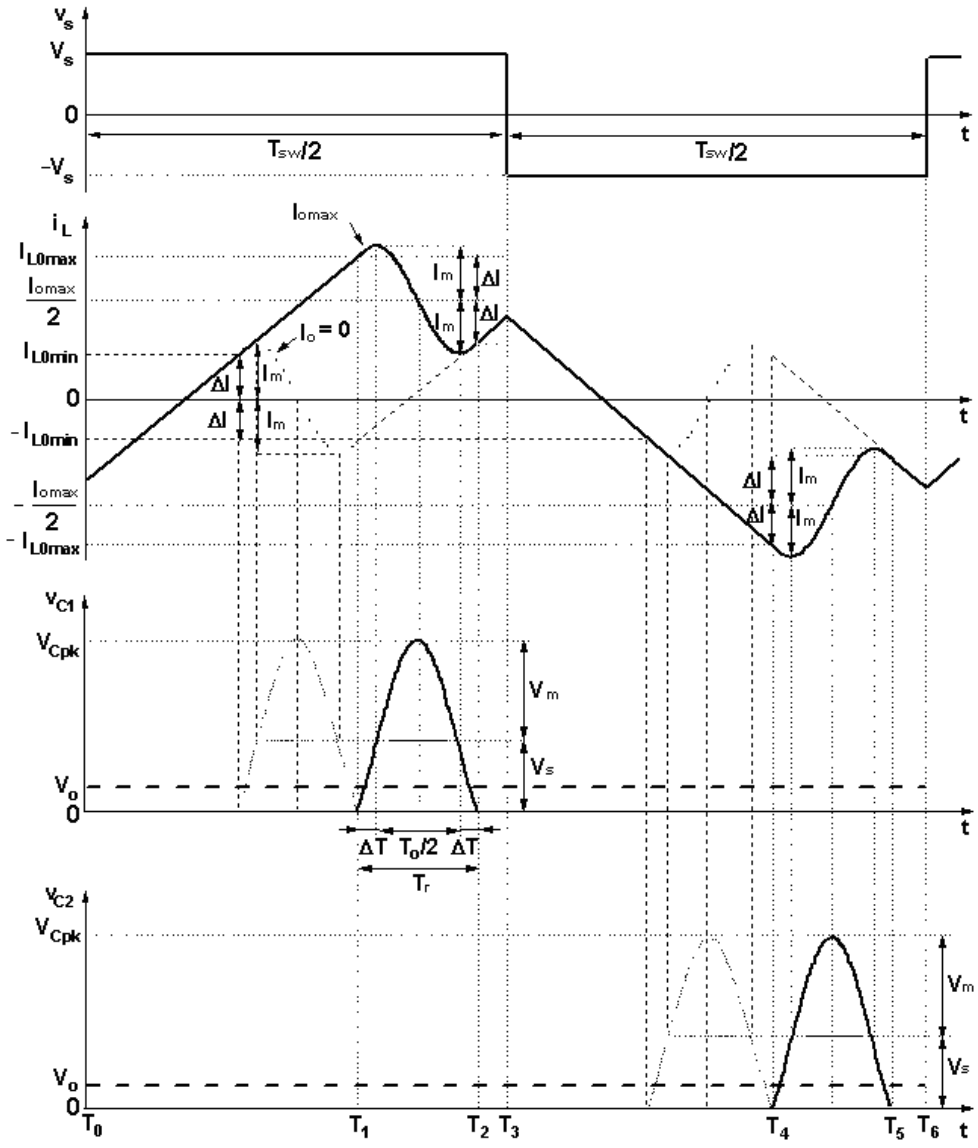


Figure 4: Key waveforms in Mode I.

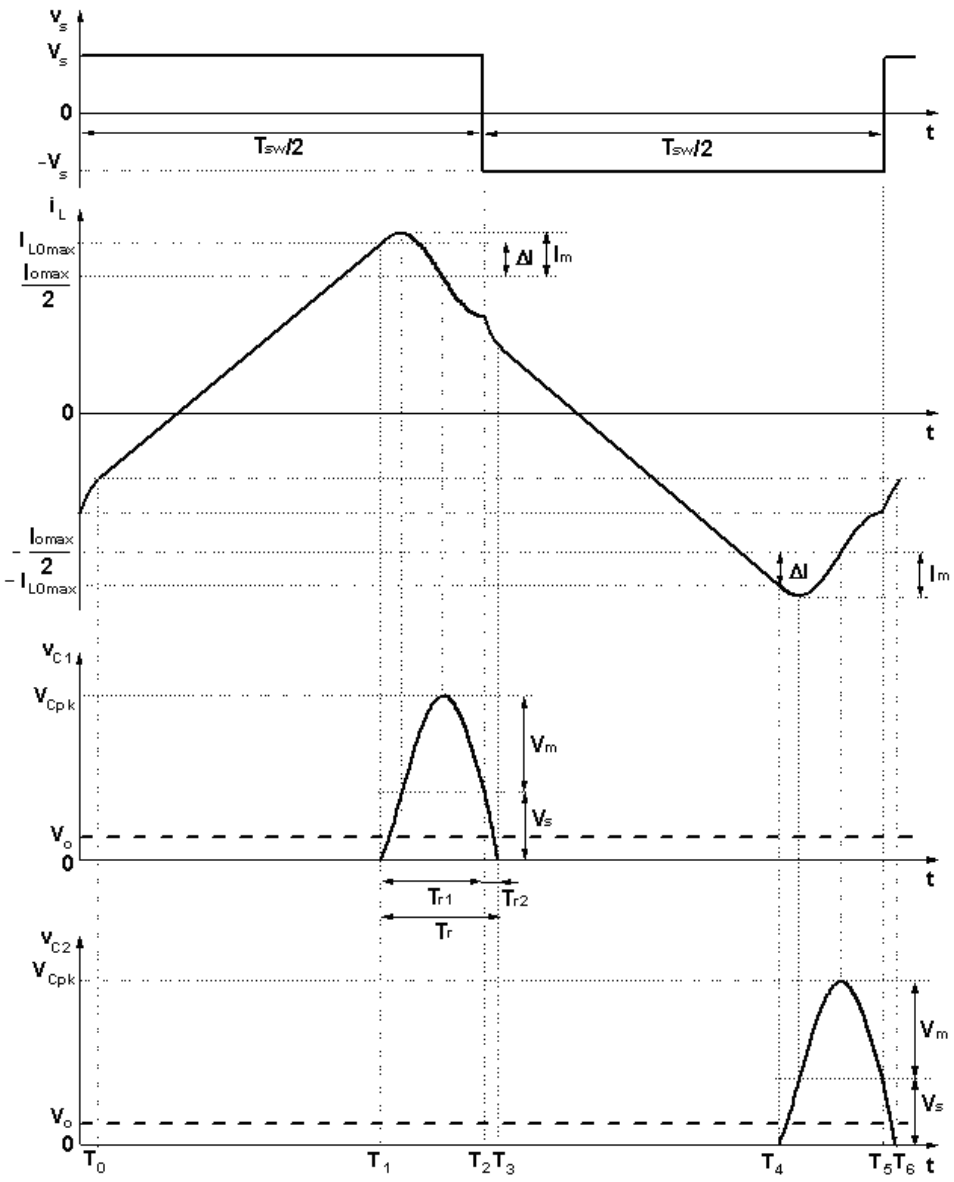


Figure 5: Key waveforms in Mode II.

Comparing the waveforms in Figs. 4 and 5, it can be seen that the phase shift of the resonant interval T_r in Fig. 5 is larger than the maximum possible phase shift in Fig. 4. In fact, by extending the operation of the circuit from Mode I in Fig. 4 to Mode II in Fig. 5, an additional phase shift can be achieved, i.e., the operation range of the circuit can be extended to larger load currents without changing the values of the resonant inductance and resonant capacitance. Because of the two resonant intervals, T_{r1} and T_{r2} in Fig. 5, the output voltage in Mode II cannot be expressed in a simple closed form such as (1) in Mode I. Nevertheless, the output voltage regulation in Mode II is similar to the output voltage regulation in Mode I.

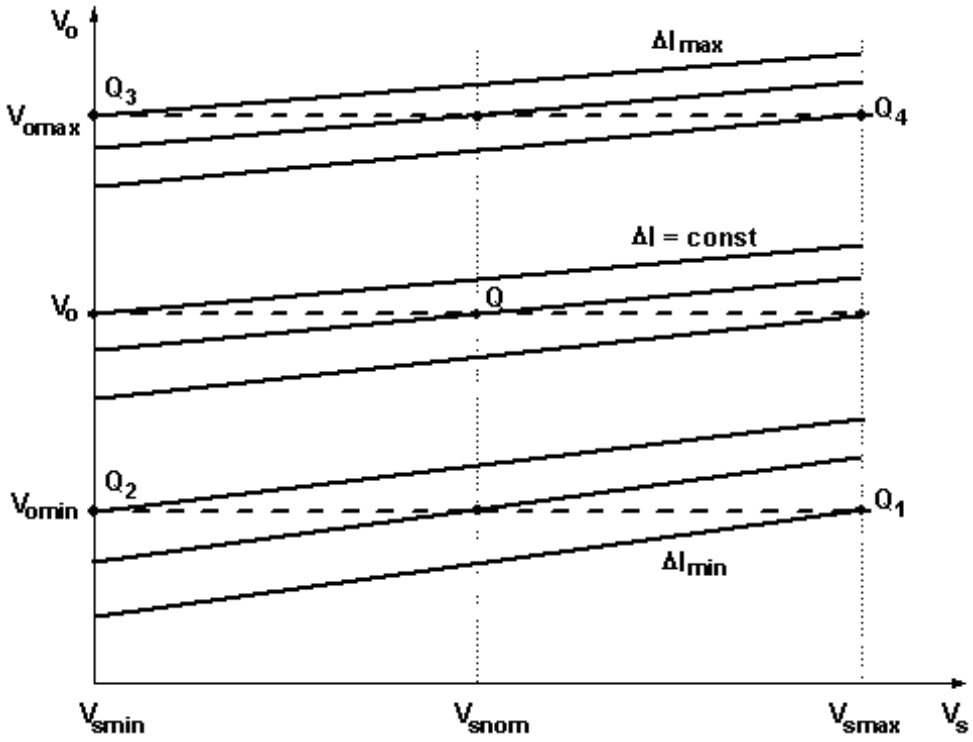


Figure 6: Output voltage regulation characteristics.

The output voltage regulation characteristics, $V_o = f(V_s)$ with ΔI used as a parameter, are presented in Fig. 6. The four extreme operating points, $Q_1 - Q_4$, are also defined in Fig. 6. From Fig. 6, the following relationships can be observed:

- at ΔI = constant,V_o increases approximately linearly with increasing V_s;
- the slope of characteristics $V_o = f(V_s)$ slightly decreases with increasing V_o;
- at V_s = constant, ΔI increases with increasing V_o;
- at V_o = constant, ΔI decreases with increasing V_s;
- $\Delta I = \Delta I_{min}$ at V_{smax} and V_{omin} (operating point Q_1);
- $\Delta I = \Delta I_{max}$ at V_{smin} and V_{omax} (operating point Q_3).

3 Implementation

The 1.8-MHz, 48-V, 130-W VRM is implemented as two 65-W VRM modules connected in parallel. The current-source property of the VRM topology (L_{ext}) allows paralleling of two or more modules without special current-sharing precautions. The two VRM modules are implemented on the same printed circuit board (PCB). Each VRM module occupies half of the PCB area.

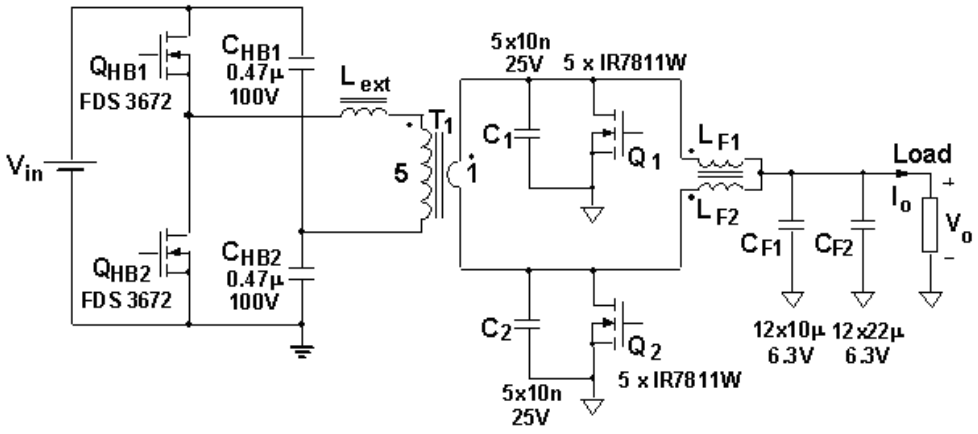


Figure 7: Simplified circuit diagram of a 1.8-MHz, 48-V, 65-W VRM module.

3.1 VRM module

The simplified circuit diagram of one 1.8-MHz, 48-V, 65-W VRM module is shown in Fig. 7. The input voltage range is 48 V ± 10% = 43.2-52.8 V. The

output voltage range is 0.95-1.7 V. The maximum load current per VRM module is 50 A at 0.95-1.3-V output voltage range, while at 1.3-1.7-V output voltage range, the maximum load current is determined by the maximum output power of 65 W.

The primary-side half-bridge inverter is implemented with FDS3672 (100 V, 7.5 A, 22 mΩ) MOSFETs from Fairchild.

Each of the secondary-side synchronous rectifiers, Q_1 and Q_2, is implemented with five parallel IRF7811W (30 V, 14 A, 9 mΩ) MOSFETs from IR.

Transformer T_1 is implemented with planar cores PC50ER14.5/6-Z from TDK and with helical windings. The primary-side magnetizing and leakage inductance of the transformer is around 25 μH and 90 nH, respectively. External resonant inductor L_{ext} is implemented with a toroidal core T37-2 from Micrometals and 9 turns, 2 strands of ϕ0.6 wire. The inductance of L_{ext} is around 330 nH. Therefore, the total primary-side resonant inductance is around 420 nH.

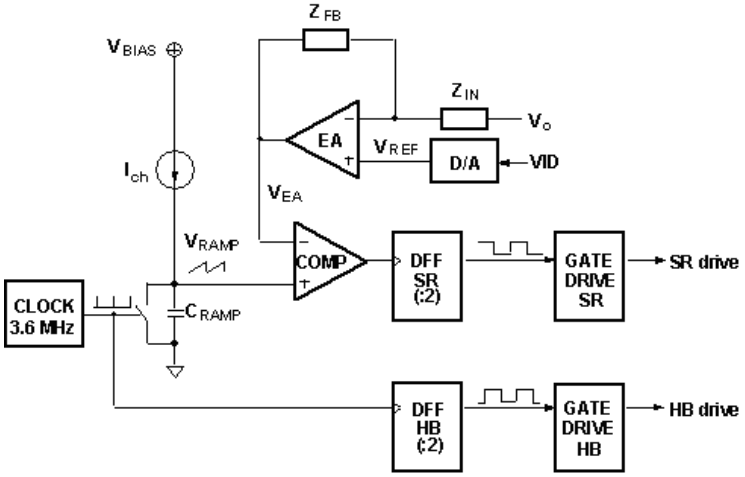


Figure 8: Functional block diagram of the control circuit.

Output-filter inductors LF1 and LF2 are coupled. They are implemented with two stacked planar EI cores 14/3.5/5 (3F3), with 1-mil air gap, and with single-turn copper bars. The inductance of each LF1 and LF2 is around 80 nH.

Finally, output-filter capacitor C_F is implemented with only surface mount ceramic capacitors. The whole output-capacitance bank is arranged in a 3x8 matrix form as shown in Fig. 10.

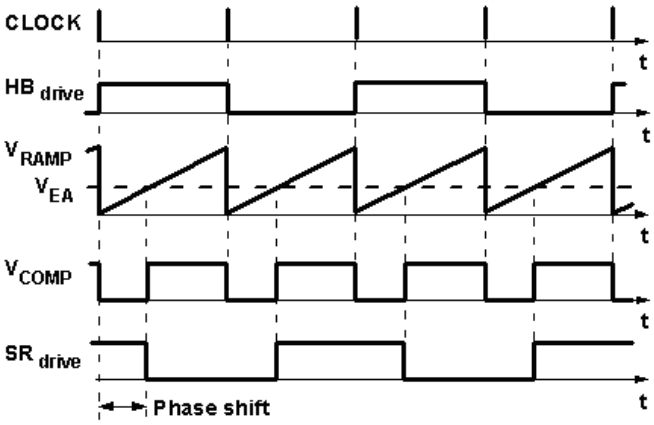


Figure 9: Key waveforms of the control circuit.

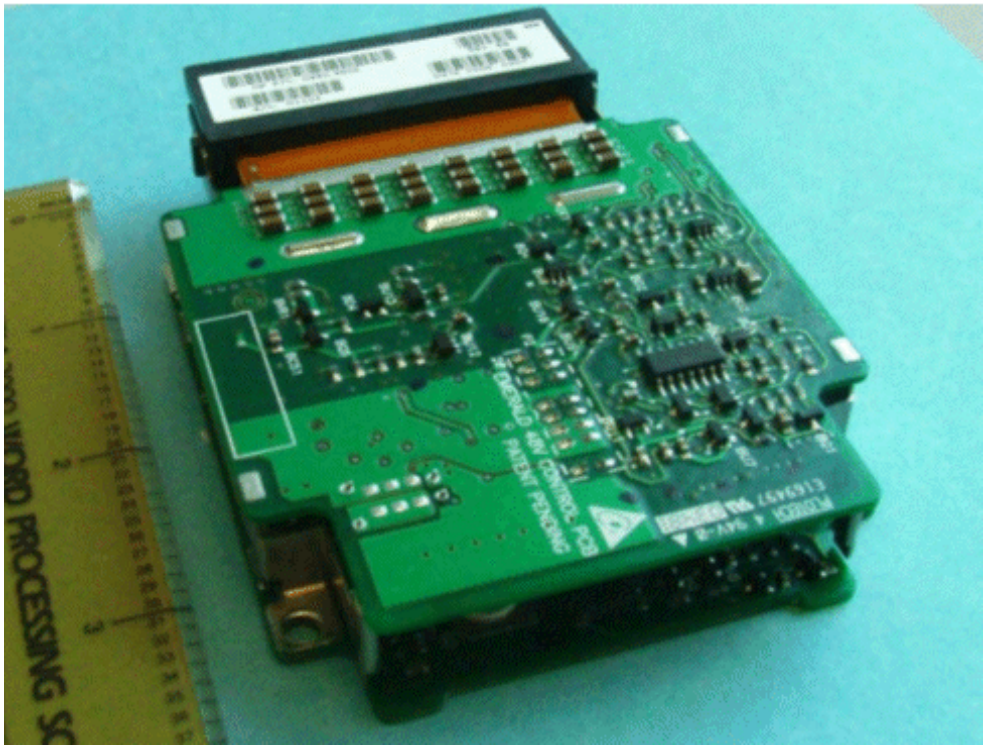


Figure 10: Experimental circuit.

3.2 Control circuit

The functional block diagram of the control circuit is shown in Fig. 8. Key waveforms are presented in Fig. 9. The clock signal in Fig 8 has a frequency equal to 3.6 MHz. The two D flip-flops, DFF SR and DFF HB, operate as frequency dividers by 2. Therefore, the frequency of the SR and HB gate drive signals is equal to 1.8 MHz. The phase-shifted control is achieved by phase shifting the SR control pulses with respect to the HB control pulses. With increasing load current, error-amplifier voltage v_{EA} increases and, through the comparator, the phase shift of the SR control pulses increases with respect to the HB control pulses.

3.3 Gate-drive circuit

The HB gate drive signals are applied to the gates of the HB switches through a gate-drive transformer. The HB switches operate with partial ZVS switching.

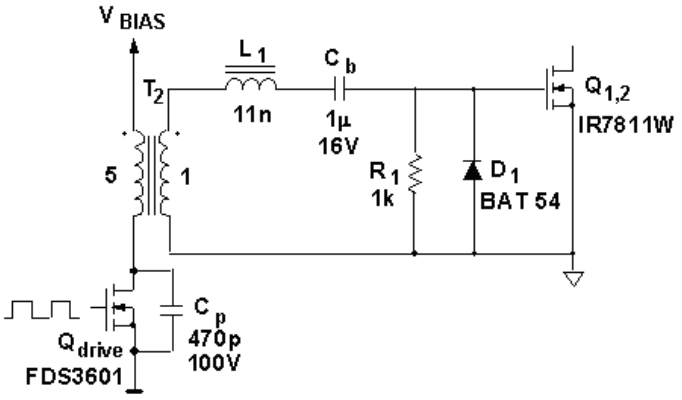


Figure 11: Resonant gate drive circuit.

The SR gate drive signals are applied to the gates of the SRs through a resonant circuit. A resonant gate drive for the SRs at 1.8-MHz switching frequency is absolutely necessary because of the large input capacitance of the SR MOSFETs. The circuit diagram of the resonant gate drive for the SRs is shown in Fig. 11. Transformer T_2 is implemented with planar cores PC50ER9.5/5-Z from TDK with 4-mil gap. The primary-side magnetizing inductance L_m is around 2 μH, while the leakage inductance L_{lk} is around 220 nH. Key waveforms are presented in Fig. 12. The waveforms in Fig. 12

are obtained for the simplified case when $L_1 = 0$ and the leakage inductance of the gate-drive transformer is neglected. The basic operation of the resonant gate drive circuit in Fig. 11 is similar to the basic operation of the main resonant converter in Fig. 2. This can be concluded by comparing the waveforms of the resonant inductor current i_{Lm} and resonant capacitor voltage v_{Cp} in Fig. 12 with the corresponding waveforms in Fig. 4. It should be noted that the total resonant capacitance in Fig. 11 consists of the capacitance C_p and the gate-source capacitance of the SR reflected to the primary side of the transformer. Bias capacitor C_b, resistor R_1, and diode D_1 in Fig. 11 form a peak detector circuit, which automatically provides a bias voltage for the SR.

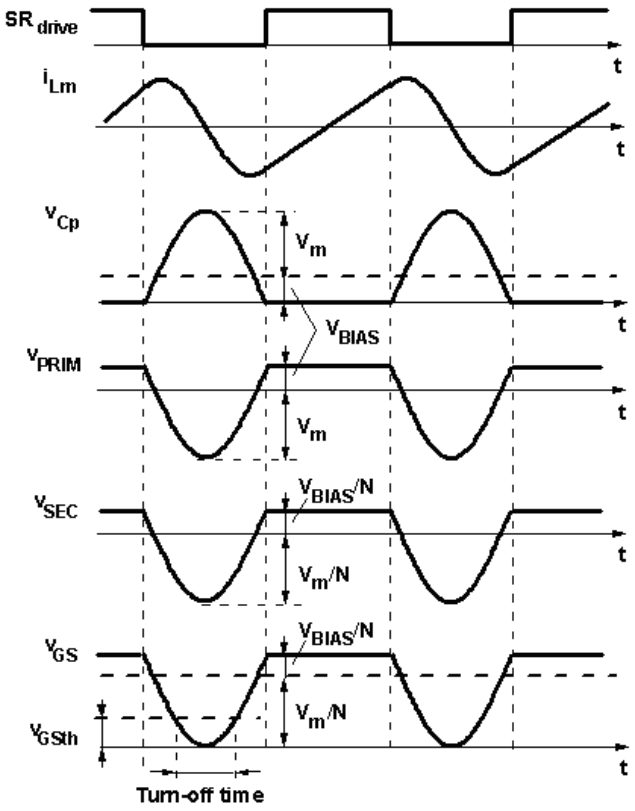


Figure 12: Key waveforms of the resonant gate drive circuit.

An improvement of the gate-drive voltage waveform can be achieved by adding inductor L_1 as shown in Fig. 11. By proper selection of induc-

tance L_1, a third harmonic can be injected in the gate-drive voltage waveform, which results in steeper edges and in an increased pulse width. Key waveforms of the improved resonant gate-drive circuit, obtained by PSPICE simulation, are presented in Fig. 13.

It should be noted that the width of the SR gate-drive pulses is critical for the proper operation of the resonant VRM. The resonant gate drive circuit in Fig. 11 generates gate-drive pulses of a constant width. However, the optimal width of the gate drive pulses varies with both the input and output voltages [5]. Therefore, with the resonant gate drive circuit in Fig. 11, optimal gate drive pulses can be obtained only for a narrow range of input and output voltages. Otherwise, if the generated pulse width is greater than the optimal pulse width, the body diode of the SR will conduct; or, if the generated pulse width is smaller than the optimal pulse width, the SR will turn on with hard switching. In both cases, the efficiency of the VRM will be reduced. Finally, if the generated pulse width is insufficient, the resonant VRM will oscillate. In applications where the reduction of the efficiency is not acceptable, instead of the RCD bias circuit in Fig. 11, a controlled bias circuit has to be employed.

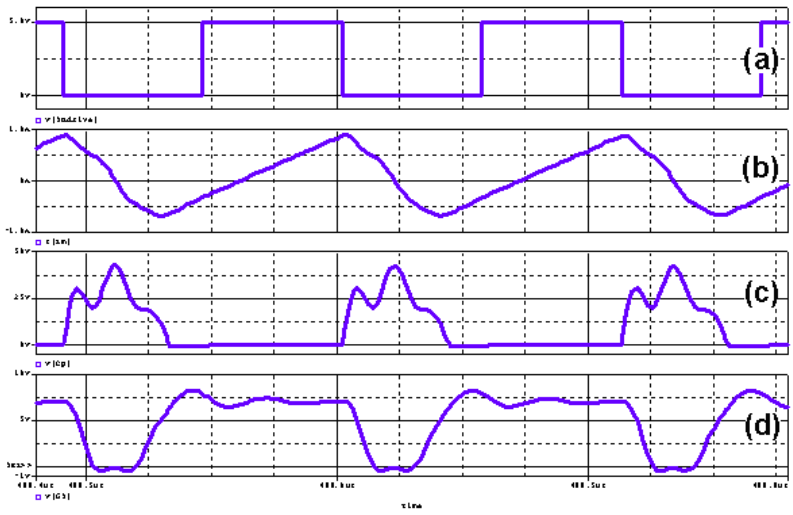


Figure 13: Key waveforms of the improved resonant gate-drive circuit obtained by PSPICE simulation: (a) SR_{drive}, (b) i_{Lm}, (c) v_{Cp}, and (d) v_{GS}.

3.4 Load-current transients

Load-current transients are specified as fast load-current transients 75-100 A and 100-75 A with a 100 A/μs slew rate, and as slow load-current transients 0-75 A and 75-0 A with a 10 A/μs slew rate. The operation of the resonant VRM at fast and slow load-current transients is illustrated in Figs. 14 and 15, respectively. The waveforms in Figs. 14 and 15 are obtained by PSPICE simulation at the nominal input voltage of 48 V and the nominal output voltage of 1.3 V. The load includes 120-μF decoupling capacitance on the microprocessor board. The connector between the VRM and the microprocessor board is modeled with 400-pH inductance and 0.6-mΩ resistance connected in series.

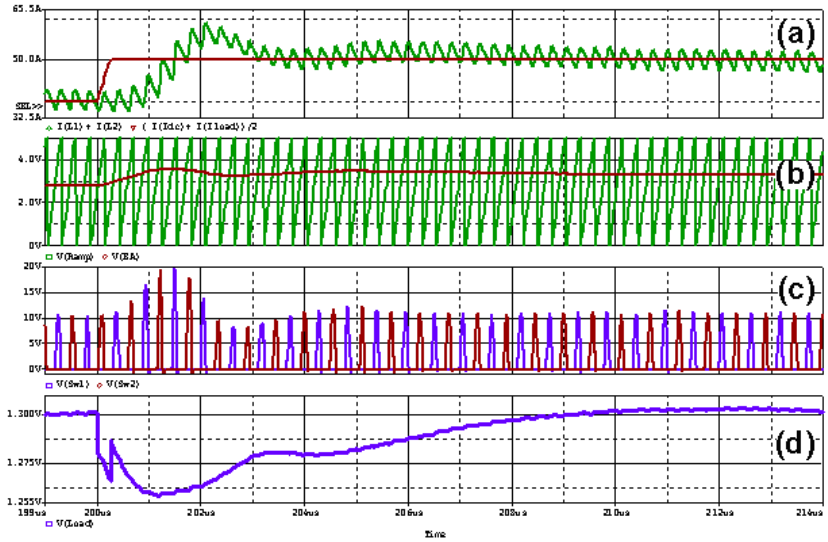


Figure 14: Operation of the resonant VRM at fast load-current transient from 75 A to 100 A with 100 A/μs slew rate, obtained by PSPICE simulation: (a) load current and output-filter inductor current $i_{LF1} + i_{LF2}$; (b) ramp voltage v_{RAMP} and error-amplifier voltage v_{EA}; (c) resonant-capacitor voltage v_{C1},v_{C2}; (d) load voltage (Time scale: 1 μs/div).

During the fast load-current transient from 75 A to 100 A, shown in Fig. 14, the load voltage exhibits an initial drop, which is caused by the equivalent series inductance (ESL) and equivalent series resistance (ESR) of the decoupling capacitance on the microprocessor board. After the initial

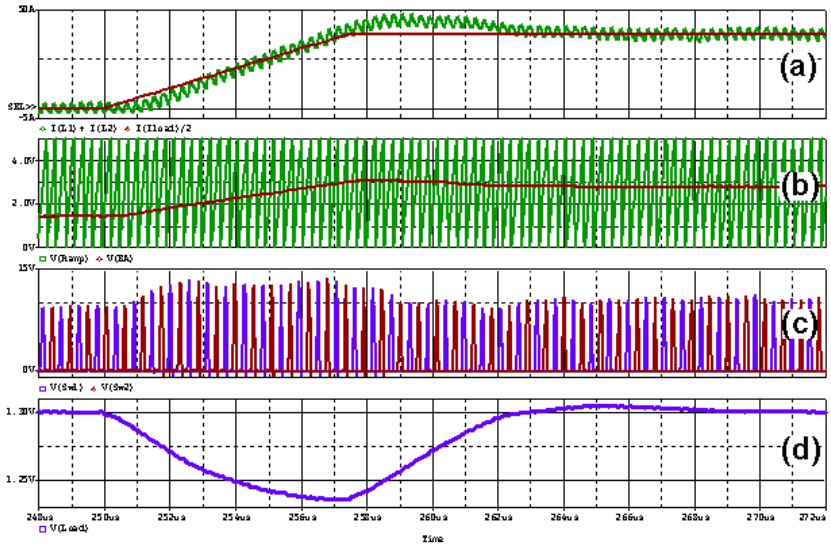


Figure 15: Operation of the resonant VRM at slow load-current transient from 0 A to 75 A with 10 A/μs slew rate, obtained by PSPICE simulation (a) load current and output-filter inductor current $i_{LF1} + i_{LF2}$; (b) ramp voltage v_{RAMP} and error-amplifier voltage v_{EA}; (c) resonant-capacitor voltage v_{C1},v_{C2}; (d) load voltage (Time scale: 1 μs/div).

drop, the load voltage is determined by the discharging of the output filter capacitor because the output filter inductor current cannot follow the fast-increasing load current. The ramp-up of the output filter inductor current is mainly determined by the speed of the control loop. The closed loop bandwidth is around 125 kHz. As shown in Fig. 14, the rise time of the output filter inductor current is around five-six clock periods. If the response of the inductor current to the step change of the load current is approximated a second-order system with the oscillation frequency close to the control loop bandwidth, the rise time of the inductor current can be approximated as a quarter of the oscillation period [6], i.e., $1/(4{\cdot}f_c) \approx 2$ μs. It should be noted that during the ramp-up of the inductor current in Fig. 14, the increased error-amplifier voltage increases the phase shift of the SR control pulses with respect to the beginning of the switching cycle, ΔI increases, and more

energy is stored in the resonant inductor. As a result, larger resonant voltage pulses are generated across the resonant capacitors C_1 and C_2. Because the average voltage across the resonant capacitors is now larger than the output voltage, the inductor current will increase.

During the slow load-current transient from 0 A to 75 A, shown in Fig. 15, the effect of the ESL and ESR of the decoupling capacitance on the microprocessor board is negligible and the load voltage is mainly determined by the discharging of the output filter capacitor. As shown in Fig. 15, the output filter inductor current closely follows the slow increasing load current. However, because of the initial delay in the control loop, the inductor current slightly lags the load current, resulting in the discharging of the output filter capacitor.

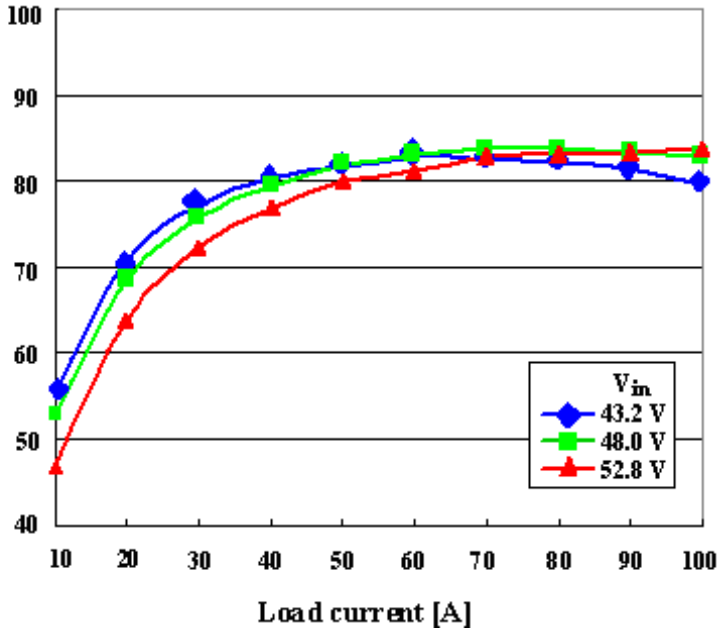


Figure 16: Efficiency measurements at nominal output voltage $V_o = 1.3$ V.

4 Experimental results

Efficiency measurements at the nominal output voltage $V_o = 1.3$ V are shown in Fig. 16. These measurements were obtained before the output connector. The resistance of the output connector is 0.5-0.6 mΩ. Therefore,

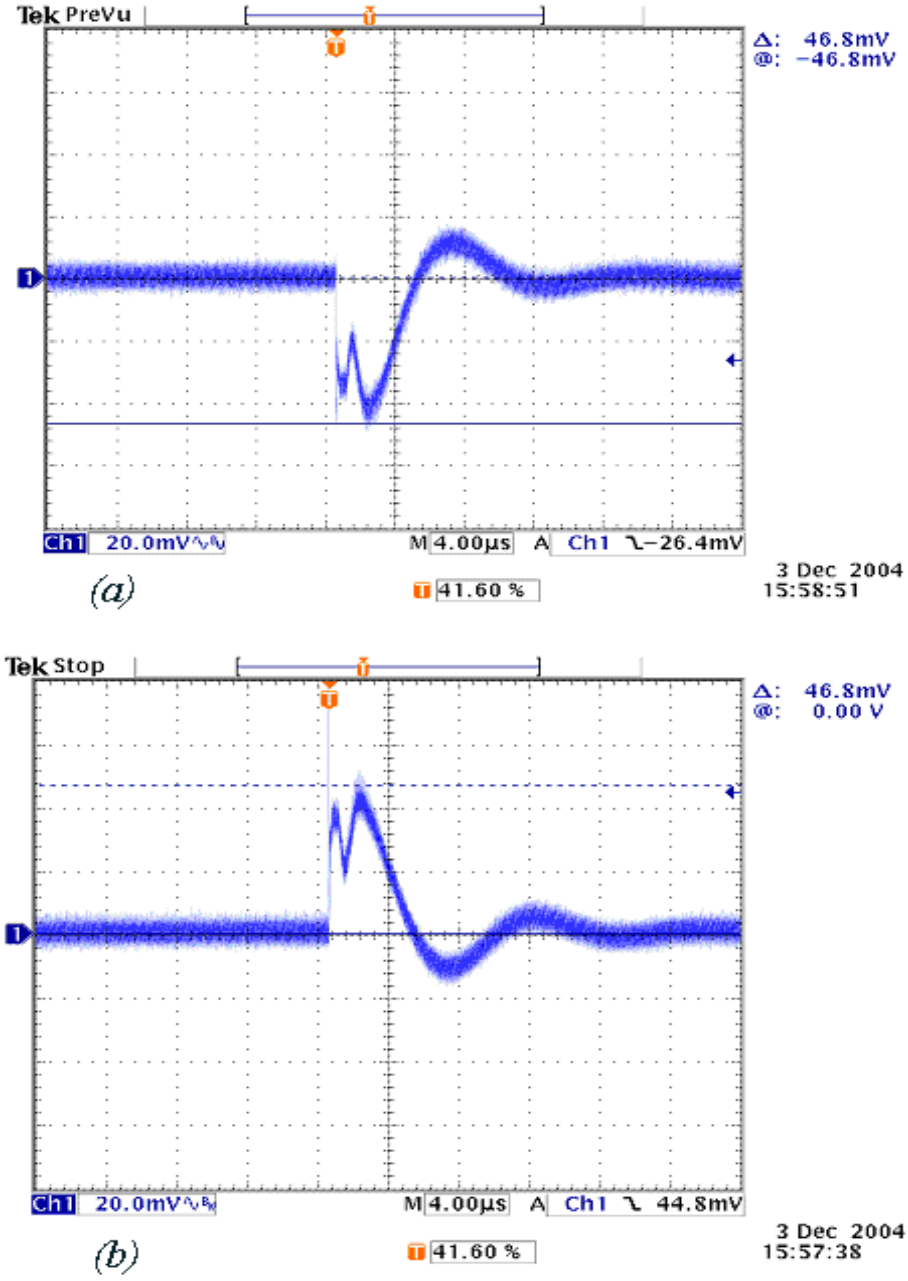


Figure 17: Output voltage waveform at fast load-current transient (a) 75-100 A and (b) 100-75 A with 100 A/μs slew rate (V_{in} = 48 V, V_o = 1.3 V).

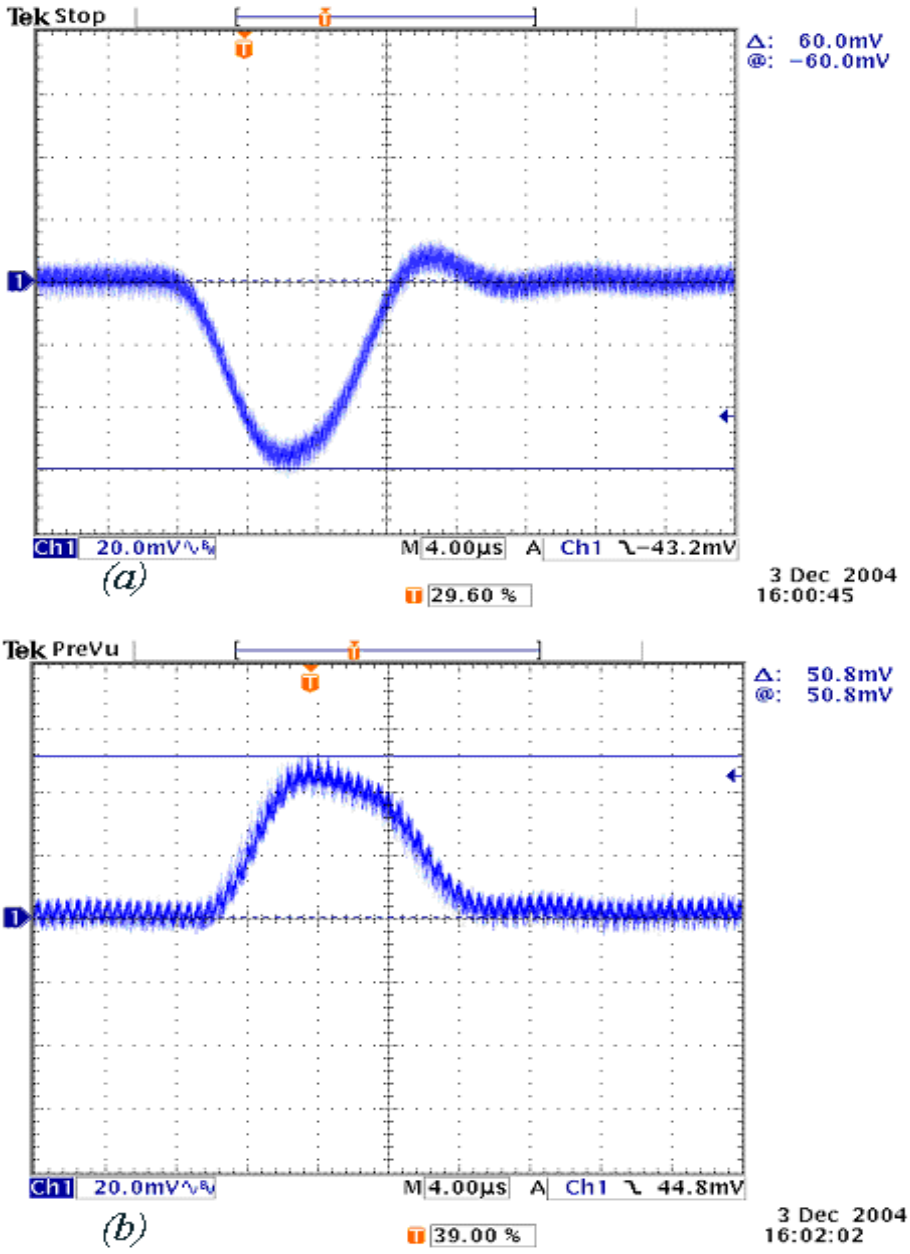


Figure 18: Output voltage waveform at slow load-current transient (a) 0-75 A and (b) 75-0 A with 10 A/μs slew rate (V_{in} = 48 V, V_o = 1.3 V).

the maximum power loss of the output connector is around 5-6 W. The efficiency at the nominal input voltage of 48 V, at 50-100 A load current is around 82-84% before the output connector and around 80-82% after the output connector.

Transient-response measurements obtained at the nominal input voltage of 48 V and the nominal output voltage of 1.3 V are shown in Figs. 17 and 18. Figures 17(a) and (b) show the output voltage waveforms at fast load-current transients 75-100 A and 100-75 A, respectively, with a 100 A/μs slew rate, while Figs. 18(a) and (b) show the output voltage waveforms at slow load-current transients 0-75 A and 75-0 A, respectively, with a 10 A/μs slew rate. The maximum deviation of the output voltage at fast and slow load-current transients is around 47 mV and 60 mV, respectively. The transient response measurements are in a good agreement with the simulation results.

5 Summary

The main features of the new high-frequency resonant converter technology with phase-shifted regulation can be summarized as follows.

- Simple isolated topology: half-bridge inverter + current-doubler rectifier with resonant synchronous rectifiers (SRs);
- Topology suitable to utilize parasitics of components and layout;
- Phase-shifted control with overlapping conduction of resonant SRs;
- Resonant gate drive of resonant SRs;
- ZVS and partial ZCS of resonant SRs;
- Only surface mount ceramic capacitors at the output;
- Fast transient response;
- Efficiency measured before the output connector around 82-84%;
- Inherent current limit protection (due to series inductance);
- Cost-effectiveness.

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