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Crosstalk noise generated by parasitic inductances in System-on-Chip VLSI interconnects

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Abstract

For System-on-Chip (SoC) using deep sub-micron technologies, semi-global and global interconnects are susceptible to crosstalk defects that may lead to mal-function and timing failures. Removal of crosstalk defects is becoming important to ensure error-free operation of an SoC. To efficiently evaluate crosstalk-defect coverage, it is necessary to understand the factors affecting this noise. In this paper, the results of study of noise induced by parasitic capacitance and inductance are observed. Crosstalk is effected by transition time of the signal; length of interconnect; distance between interconnects; size of driver and receiver; pattern of input; direction of flow of signal; and clock skew. This work is based on simulating interconnects with parameters obtained from 0.13μm process. The types of noise addressed are overshoot; undershoot and oscillatory noise. It is observed that presence of inductive effects can seriously hamper the functioning of the chip. In conclusion, the impact of the above observations on tests of inductance induced noise is summarized.

Keywords: VLSI, Crosstalk, RLC interconnect, simulation, over and under shoots.

1 Introduction

The feature size of integrated circuits has been aggressively reduced in the pursuit of improved speed, power, silicon area and cost characteristics [1]. Semiconductor technologies with feature sizes of several tens of nanometers are currently in development. As per, International Technology Roadmap for Semiconductors (ITRS) [2], the future nanometer scale circuits will contain more than a billion transistors and operate at clock speeds well over 10GHz. Distributing robust and reliable power and ground; clock; data and address; and other control signals through interconnects in such a high-speed, high-complexity environment, is a challenging task.

The performance of a high-speed chip is highly dependent on the interconnects, which connect different macro cells within a VLSI chip. With ever-growing length of interconnects and clock frequency on a chip, the effects of interconnects cannot be restricted to RC models. The importance of on-chip inductance is continuously increasing with faster on-chip rise times, wider wires, and the introduction of new materials for low resistance interconnects. It has become well accepted that interconnect delay dominates gate delay in current deep sub micrometer VLSI circuits [1-9]. With the continuous scaling of technology and increased die area, this behavior is expected to continue. Thus interconnect designing has emerged as an important research area.

Wide wires are frequently encountered in global and semi-global interconnects in upper metal layers. These wires are low resistive lines that can exhibit significant inductive effects. Due to presence of these inductive effects, the new generation VLSI designers have been forced to model the interconnects as distributed RLC transmission lines [10-11]. These RLC transmission line when running parallel to each other have capacitive and inductive coupling, which makes the design of interconnects even more important in terms of crosstalk. Much of the research efforts till date have been directed towards reducing delay and power dissipation only [12-20]. In a modern interconnect design, the interconnects in an adjacent metal layers are kept orthogonal to each other. This is done to reduce crosstalk as far as possible. But with growing interconnect density and reduced chip size, even the non-adjacent interconnects exhibit significant coupling effects. These coupling effects are significantly dependent on length of interconnects, distance between them, transition time of the input and the pattern of input.

On-chip inductance induced noise to signal ratio is increasing because of the increase in switching speed; decrease in separation between interconnects and decrease in noise margins of devices. The impact of this noise, such as

oscillation, overshoots and undershoots, on chip's performance is thus of concern in design. The effect of a crosstalk induced overshoot and undershoot generated at a noise-site can propagate false switching and create a logic error. The false switching occurs when the magnitude of overshoot or undershoot is beyond the threshold of the gate. The peak overshoot and undershoot generated at a noise-site can also wear out the thin gate oxide layer resulting in permanent failure of the chip. This problem will be significant as the feature size of transistor reduces with advancement of technology.

Extraction of exact values of capacitance and inductance induced noise for an interconnect is a challenging task. For an on-chip interconnect, the different behavior of capacitive and inductive noise must be taken into consideration. Since electrostatic interaction between wires is very short range, consideration of only nearest neighbors provides sufficient accuracy for capacitive coupled noise. Unlike an electric field, a magnetic field has a long range interaction. Therefore in inductive noise extraction not only nearest neighbors but also many distant wires must be considered. As a consequence, defining current loops or finding return paths becomes a major challenge in inductive noise modeling. Since magnetic fields have a much longer spatial range compared to that of electric fields, in practical high-performance ICs containing several layers of densely packed interconnects, the inductive noise are sensitive to even distant variations in the interconnect topology [1]. Secondly, uncertainties in the termination of the neighboring wires can significantly affect the signal return path and return current distributions and therefore the effective inductive noise. Also, accurate estimation of the effective inductive noise estimation requires details of the 3-D interconnect geometry and layout, technology etc., and the current distributions and switching activities of the wires, which are difficult to predict. Moreover, at high frequencies the line inductance parameters are also dependent on the frequency of operation. These are the added complexities for the designers involved in analyzing the behavior of the interconnects. Without involving in the complexities of a high-performance chip, this paper shows the prominent factors such as edge rate, length and pattern of inputs affecting the noise.

In this paper we present simulation results with a focus on crosstalk and oscillatory noise. Though the observations held here can be applied to different areas of VLSI design, we are primarily concerned with their implications on test generation. We study the impact of transition time (edge rate); length of interconnect; and pattern of input on the aggressor and victim line, on the magnitude of noise.

2 Experimental setup

For our studies through SPICE simulations, we use a 0.13μm technology with copper interconnects process. The power supply (Vdd) is taken as 1.5V, the threshold voltages are roughly 10% of Vdd. It is assumed that there are several metal layers available for the interconnects. Each interconnect is 2μm wide. The thickness of interconnect is 0.68μm. The interconnect spacing is 0.24μm. It is well accepted that simulations of a distributed RLC model of an interconnect matches more accurately the actual behavior in comparison to a lumped RLC model. A distributed RLC model of an interconnect, known as the transmission line model, becomes the most accurate approximation of the actual behavior [1]. The transmission line is therefore modeled by 20 distributed lumps. The capacitance and inductance values are obtained from [21-23]. In this paper, we primarily study the noise for transition time varying from 1ps to 25ps. The interconnect length is varied from 1mm to 10mm. These parameters are varied for four different cases of stimulations to aggressor and victim lines (Fig. 1) *viz.*

(I) V_A (input at aggressor node A) and V_B (input at victim node B) switching in same direction from high to low.

(II) V_A and V_B switching in opposite direction.

(III) V_A switching from high to low and V_B at static low

(IV) V_A switching from high to low and V_B at static high

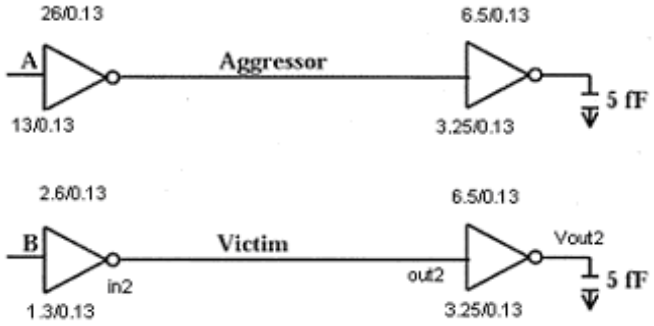

Figure 1: Circuit used to study crosstalk overshoot and undershoot.

A transmission line model is used for the simulation of circuit (Fig. 2). An example of how interconnect parameter matrices are formed for the case of two interconnects is shown in Fig. 3. R_A, C_A, and L_A are the resistance, capacitance, and inductance per unit length for line A, and R_B, C_B, and L_B are the same parameters for line B. C_{AB} and L_{AB} are the mutual capacitances and inductances, respectively. The aggressor and victim lines driver and receiver sizes are mentioned in Fig. 1. The W/L ratio above and below the gate in Fig. 1 refers to PMOS and NMOS transistor respectively. The channel length is 0.13μm for all transistors. The experimental set up measures for maximum and minimum level of magnitude at three nodes i.e. input of transmission line *in2*, output of transmission line *out2* and at load capacitance of receiver *Vout2*.

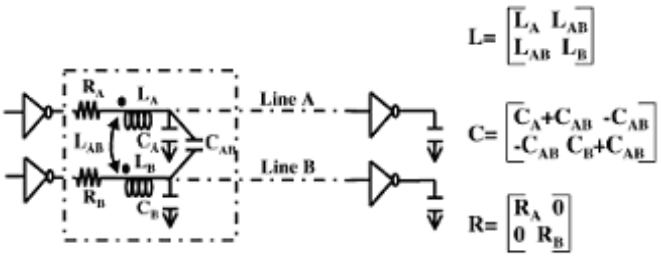

Figure 2: Circuit model and parameter matrices.

$$R = \begin{bmatrix} 12500 & 0 \\ 0 & 12500 \end{bmatrix}, \quad L = \begin{bmatrix} 1.722\mu & 1.4\mu \\ 1.4\mu & 1.722\mu \end{bmatrix}, \quad C = \begin{bmatrix} 190p & -64p \\ -64p & 190p \end{bmatrix}$$

Figure 3: Interconnect parameters.

3 Signal transition time/edge rate

Firstly, the impact of edge rate on the crosstalk overshoot and undershoot is considered. The maximum and minimum level of noise magnitude at victim's *in2*, *out2* and *Vout2* node is observed. An interconnect of length

3mm is chosen to demonstrate crosstalk behavior. The input at aggressor switches from logic high to low, whereas for simplicity of observation of crosstalk, the victim is kept static at either logic low or high. The victim's maximum and minimum node voltages for varying transition time from 1ps to 25ps for both Cases (III and IV) are shown in Figures 4 and 5. The maximum and minimum magnitude of voltage for three nodes *in2*, *out2* and *Vout2* are shown in figure by postfixing '*max*' and '*min*' to the respective node names. It is observed that the maximum and minimum magnitude of the node voltages change non-monotonically with edge-rate. The severity of crosstalk becomes enormous as transition time becomes very low.

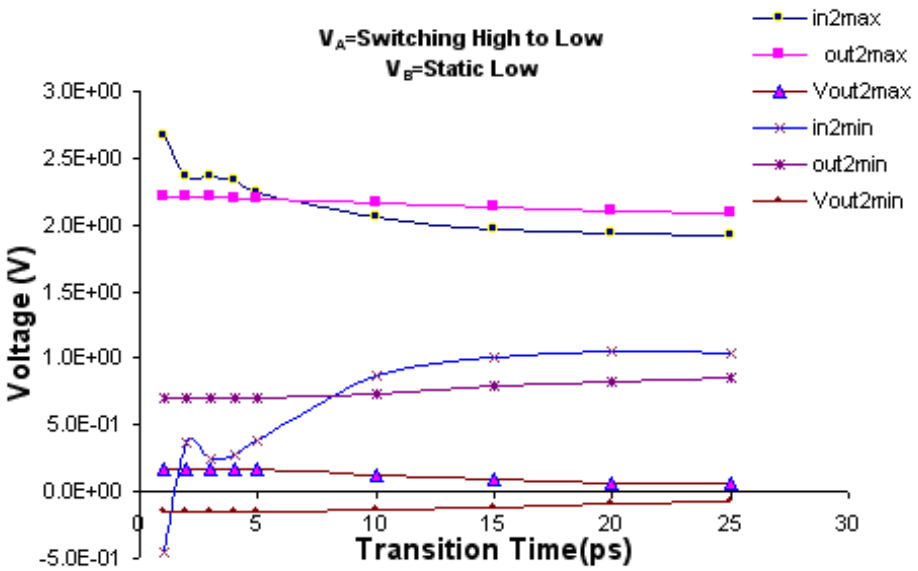

Figure 4: Node voltages *vs* transition time for an interconnect length 3mm (Case III).

Following are the observations:

1. When the input to the victim is static low (Case III) the nodes viz. *in2*, *out2* and *Vout2* in absence of crosstalk are held at logic state high, high and low respectively. When the aggressor switches from high to low, the peak overshoot due to crosstalk at the near end of the victim transmission line i.e. *in2* is quite severe as compared to other nodes (Fig. 4). The overshoot results in negative conductance for the

victim's driver PMOS, whereas its NMOS will be subjected to very high electric field between its drain and source i.e. channel length region, which will wear out the transistor and lead to catastrophe. Similar observations are made for peak undershoots. Under crosstalk effect for peak undershoot, the near end node *in2* voltage is forced to negative value for an edge rate of 1ps, which otherwise in normal operation without crosstalk should have been logic high. This clearly shows that crosstalk effect can be highly detrimental as far as logics are concerned.

2. The peak over and under shoots noise magnitude at *Vout2* for transition time from 1ps to 5ps is in a range comparable to the threshold voltage of NMOS and PMOS transistor respectively.

3. The peak undershoot voltage *out2min* reaches a voltage level less than logic threshold of the gate for an edge rate less than 10ps. The node *out2* voltage must have been otherwise held at logic high level. Thus, due to crosstalk there will be false switching which in turn results in logic error. Many analysis consider only peak voltages and neglect undershoot. The observation made in this paper shows that even peak undershoot can be equally responsible for logic failure of a circuit.

4. The peak overshoot at far end of the transmission line i.e. *out2max* does not pose much problems and remains approximately constant with respect to edge rate. The reason behind it is that the overshoot dies out due attenuation as it traverses through the interconnect.

5. When the input to the victim is static high (Case IV) the nodes viz. *in2*, *out2* and *Vout2* in absence of crosstalk are held at logic state low, low and high respectively. Node *in2* i.e. near end of the transmission line is most severely affected by the crosstalk. Both peak over and under shoots reaches a level of Vdd and -Vdd respectively at an edge rate of 1ps (Fig. 5). The -Vdd level will force PMOS channel electric field to double the value which it normally operates in. Coupled with velocity saturation effects at deep submicron level, crosstalk effects will pose serious problem in the functioning of the CMOS gate. Thus peak undershoots cannot be neglected in the future analysis.

6. For Case IV input, *out2max* voltage is observed to be at a level comparable to the logic threshold of the receiver gate. *Vout2max* and *Vout2min* do not pose enough problems since even at lowest edge rate the peak over and under shoots are around the supply voltage.

Even though such edge-rates are very fast and not seen in current technologies, such fast edge-rates will be possible in future technologies. Since other parameters will also change in future technologies, whether this non-monotonic effect becomes significant or remains an uncommon effect can only be verified when data from future processes are available.

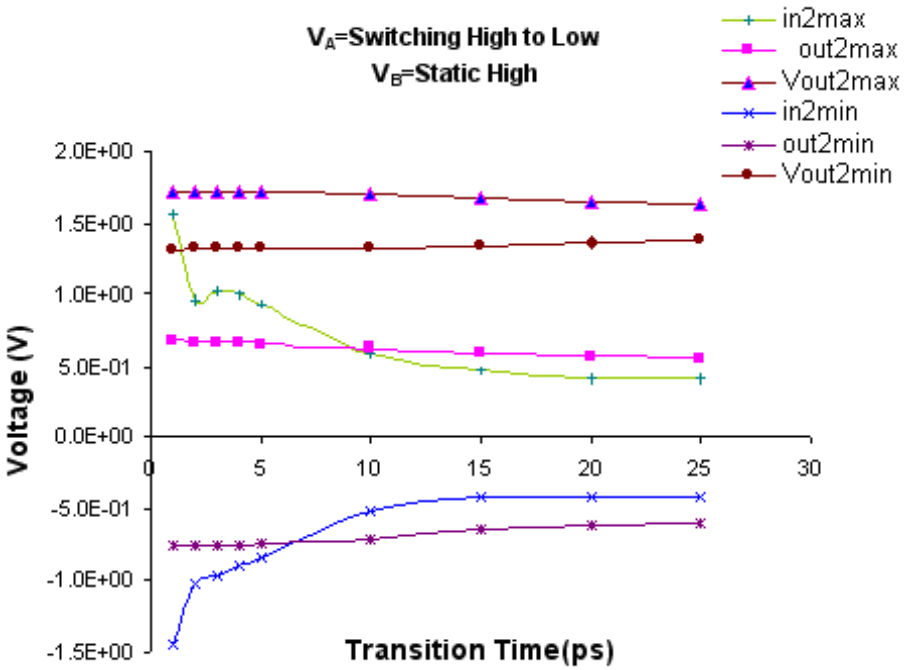

Figure 5: Node voltages *vs* transition time for an interconnect length 3mm (Case IV).

4 Interconnect length

The impact of interconnect length on crosstalk is now studied. We are primarily interested in global and semi-global interconnects. The interconnect lengths that come in this range are from 1mm to 10mm.

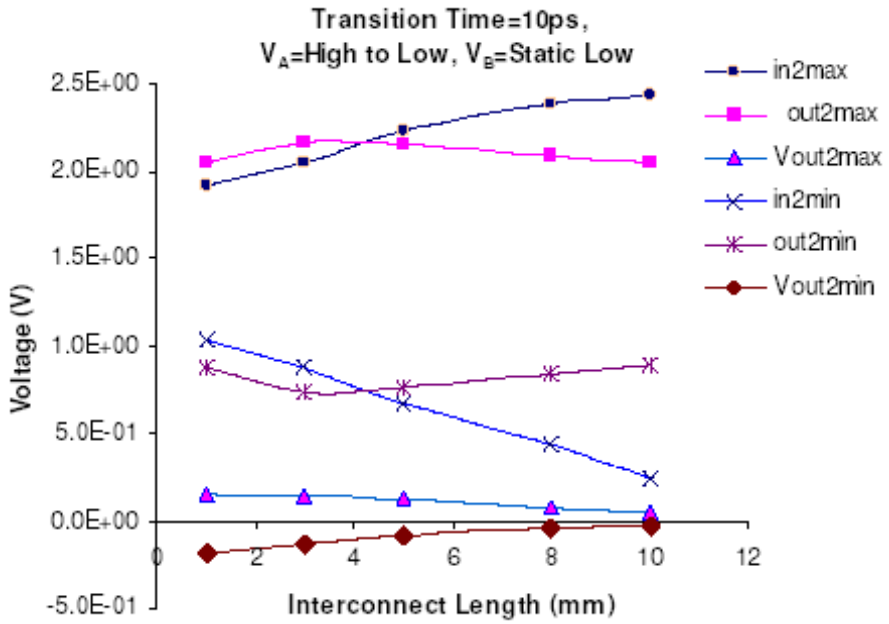

Figure 6: Node voltages *vs* interconnect length for transition time of 10ps (Case III).

Following are the observations:

1. It is observed that maximum and minimum crosstalk magnitude level, *in2max* and *in2min* at node *in2* increases for Case III (Fig. 6) and Case IV (Fig. 7) respectively, as the length of interconnect is increased. This behavior is observed due to higher inductive effects seen by the node as line becomes longer.

2. Overshoot (*out2max*) and undershoot (*out2min*) voltages at node *out2*, first increases and then decreases. Matching of characteristic impedance of transmission line at driver and load end plays an important role in determination of maximum crosstalk. For the given example the crosstalk level attains its maximum magnitude for peak over and under shoot at an interconnect length of 3mm. For the lengths longer and shorter than 3mm the magnitude of crosstalk decreases. The peak that occurs at an interconnect length of 3mm is more than seven times the threshold voltage of transistor and is roughly equal to logic threshold of the gate.

3. The overshoot (*Vout2max*) and undershoot (*Vout2min*) voltage at node *Vout2* decreases non-monotonically as the length of interconnect increases. The overall noise is reduced due to the signal conditioning effects of the receiver gate. As the size of the receiver gate is increased the noise effects will be substantially reduced.

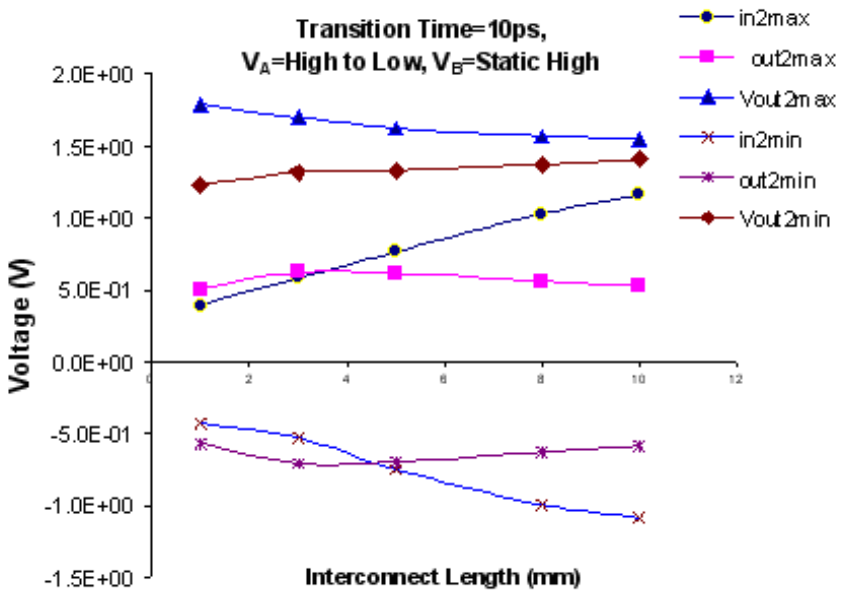

Figure 7: Node voltages *vs* interconnect length for transition time of 10ps (Case IV).

5 Switching pattern on aggressor and victim lines

The impact of switching pattern on aggressor and victim lines is quite significant on crosstalk over and under shoots. The Partial Differential Equations (PDE) that describe two coupled distributed *rlc* interconnects are given by [24]

$$\frac{\partial^2}{\partial x^2}V_A(x,t) = r(c + c_{AB}\frac{\partial}{\partial t}V_A(x,t) - rc_{AB}\frac{\partial}{\partial t}V_B(x,t) \quad (1)$$
$$+ [l_s(c + c_{AB} - l_{AB}c_{AB}]\,\frac{\partial^2}{\partial t^2}V_A(x,t) + [l_{AB}(c + c_{AB} - lc_{AB}]\,\frac{\partial^2}{\partial t^2}V_B(x,t)$$

$$\frac{\partial^2}{\partial x^2}V_B(x,t) = r(c + c_{AB}\frac{\partial}{\partial t}V_B(x,t) - rc_{AB}\frac{\partial}{\partial t}V_A(x,t) \quad (2)$$
$$+ [l_s(c + c_{AB} - l_{AB}c_{AB}]\,\frac{\partial^2}{\partial t^2}V_B(x,t) + [l_{AB}(c + c_{AB} - lc_{AB}]\,\frac{\partial^2}{\partial t^2}V_A(x,t)$$

where

V_B transient voltage along an active line (line B);

V_A transient voltage along victim line (line A);

r resistance per unit length of line A and B;

c line-to-ground capacitance (C_A and C_B) per unit length;

c_{AB} line-to-line capacitance (C_{AB}) per unit length;

l self-inductance (L_A and L_B) per unit length;

l_{AB} mutual inductance between the two conductors (L_{AB}) per unit length.

Adding and subtracting equations (1) and (2) gives the following set of decoupled PDEs:

$$\frac{\partial^2}{\partial x^2}V_+(x,t) = (l + l_{AB})c\frac{\partial^2}{\partial t^2}V_+(x,t) + rc\frac{\partial}{\partial t}V_+(x,t) \quad (3)$$

$$\frac{\partial^2}{\partial x^2}V_-(x,t) = (l - l_{AB})(c + 2c_{AB})\frac{\partial^2}{\partial t^2}V_-(x,t) + r(c + 2c_{AB})\frac{\partial}{\partial t}V_-(x,t) \quad (4)$$

where $V_+ = V_A + V_B$ (Plus Mode) and $V_- = V_A - V_B$ (Minus Mode).

As per [24] there are two modes of propagation in a coupled RLC transmission line i.e. plus and minus modes. The plus and minus modes have physical interpretations as being the solutions to the coupled line configuration with two different initial conditions. The plus mode, for example, has the interpretation that it is the solution to the voltage of either line when both are excited simultaneously (Case I). The effective capacitance of the plus mode is, therefore, the line-to-ground capacitance because by definition the potential between the lines is zero. The currents in this plus

configuration are in the same direction; therefore, the magnetic flux emanating from each line is in the same direction in the orthogonal surface linking each conductor to the ground plane. For this configuration, the effective flux linkage of each line is increased which produces a higher effective inductance (self-inductance plus the mutual inductance) for the plus mode. The minus mode is the solution to the transient response of the active line when the adjacent line is switching with opposite polarity (Case II). Because of the Miller effect, the mutual capacitance is effectively twice its original value. The minus mode has an effective capacitance equal to the line-to-ground capacitance plus *twice* the mutual capacitance. In addition, the currents in this configuration are equal in magnitude and opposite in direction. The magnetic fluxes emanating from each line are in opposite direction. The effective flux linkage of each line is, therefore, reduced which produces an effectively lower inductance. The minus mode has an effective inductance equal to the self-inductance minus the mutual inductance.

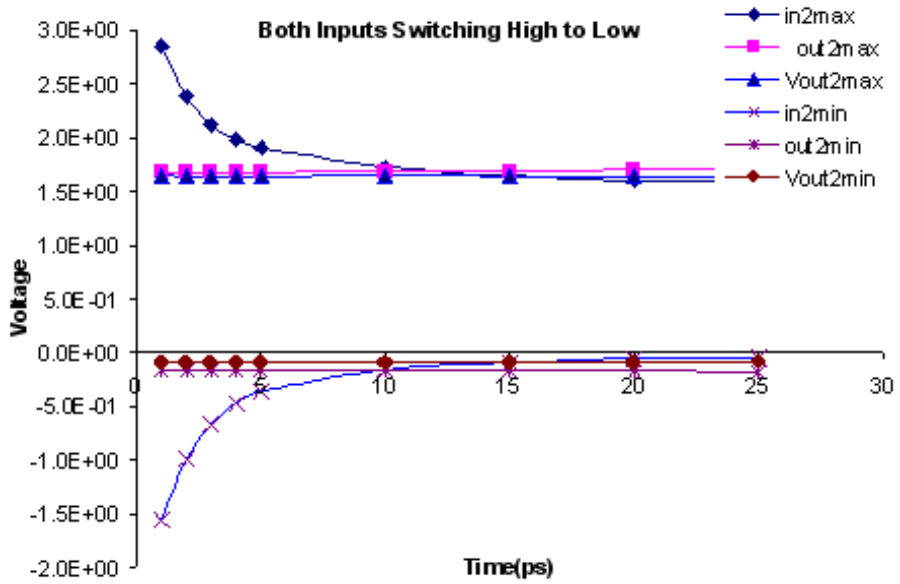

Figure 8: Node voltages *vs* transition time for an interconnect length 5mm (Case I).

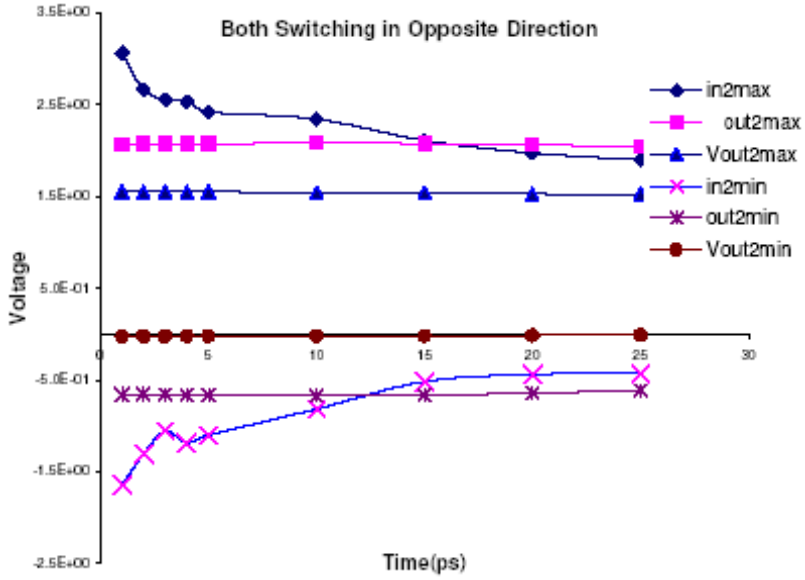

Figure 9: Node voltages *vs* transition time for an interconnect length 5mm (Case II).

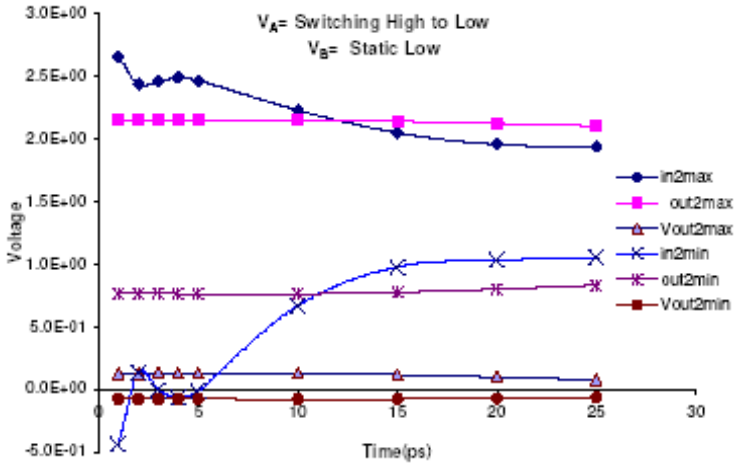

Figure 10: Node voltages *vs* transition time for an interconnect length 5mm (Case III).

We show the level of overshoot and undershoot results for all possible switching patterns (Cases I to IV). An interconnect of length 5mm is stimulated by a signal having transition time from 1ps to 25ps. The maximum and minimum level of signal at nodes *in2*, *out2* and *Vout2* are shown respectively for Cases I to IV in Fig. 8 to Fig. 11. It is observed that maximum over and under shoots level for node *in2* and *out2* occur for Case II, where the input to aggressor and victim line switches in opposite direction. For this case, the effective coupled capacitance is doubled and the coupled inductance is reduced. In Case-I, although the coupled capacitance is reduced to zero, but the inductive coupling is strong enough to produce comparable over and under shoots. And thus it is shown that the inductive effects which were earlier neglected, can become a major concern for an interconnect designer. For Cases III and IV inductive and capacitive coupling both play their respective roles to produce over and under shoots.

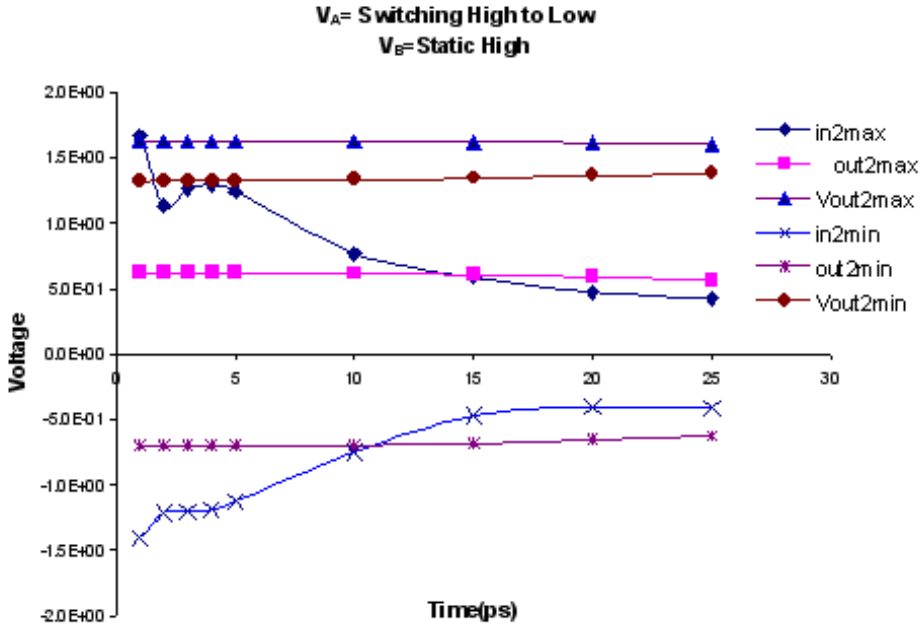

Figure 11: Node voltages *vs* transition time for an interconnect length 5mm (Case IV).

6 Conclusion

The crosstalk noise due to presence of self and mutual parasitic inductance and capacitance is studied. An interpretation is drawn from simulation results that in the worst case of an overshoot or undershoot, false switching and/or gate oxide wear out can occur which may result in malfunctioning of the chip. Such noise may cause an erroneous value to be stored in latches/ flip-flops. It has been argued by others that inductance induced problems are most pronounced in long buses, and that there is no need to study such noise in medium length interconnects. We observed in section-III that, in current technology, interconnects in semi-global lengths are long enough to give rise to significant crosstalk induced errors. Therefore, inductance induced noise should be considered during test generation for combinational blocks with medium length lines. We observed that the crosstalk noise takes its worst form for low transition time; medium/ long length interconnect; aggressor and victim line switching in opposite direction. Thus, a test generator should not only assign logic values on aggressor and victim lines to create worst case noise effects, but also assign appropriate logic values on lines adjacent to the aggressor and victim.

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